An Improved Power Quality IHQRR-BIFRED Converter Fed BLDC Motor Drive

Bhim Singh* and Vashist Bist†

*†Dept. of Electrical Engineering, Indian Institute of Technology Delhi, New Delhi, India

Abstract

This paper presents an IHQRR (Integrated High Quality Rectifier Regulator) BIFRED (Boost Integrated Flyback Rectifier Energy Storage DC-DC) converter fed BLDC (Brushless DC) motor drive. A reduced sensor topology is derived by utilizing a BIFRED converter to operate in a dual DCM (Discontinuous Conduction Mode) and thus utilizing a voltage follower approach for PFC (Power Factor Correction) and voltage control. A new approach of speed control is proposed using a single voltage sensor. The speed of the BLDC motor drive is controlled by varying the DC link voltage of the front end converter. Moreover, a fundamental frequency switching of the VSI’s (Voltage Source Inverter) switches are used for the electronic commutation of BLDC motor which reduces the switching losses in the VSI. The proposed drive is designed for a wide range of speed control with improved power quality at the AC mains within the recommended limits by international power quality standards such as IEC 61000-3-2.

Key words: BIFRED Converter, BLDC motor, DCM, IHQRR, PFC, Power Quality.

I. INTRODUCTION

Research on PFC (Power Factor Corrected) converters for attaining an improved power quality at the AC mains becomes popular after the stringent limits imposed by the international power quality standards such as IEEE-519 and IEC-61000-3-2 [1, 2]. Power quality indices such as PF (Power Factor), DPF (Displacement Power Factor), THD (Total Harmonic Distortion) and CF (Crest Factor) of the supply current are limited within certain prescribed value by these standards for different class of equipments [1, 2]. For drive applications i.e. class-A equipments (under 600 W, <16 A per phase), a power factor above 0.98 and THD of supply current below 5% is considered to be a well acceptable limit to meet the requirement of IEC-61000-3-2 [2].

BLDC (Brushless DC) motors are becoming popular for the development of any low and medium power equipment. It offers many advantages including high torque and watt per unit weight, high efficiency, high reliability, low noise levels and long lifetime (since no brush and commutator are used) with reduced EMI (Electromagnetic Interference) problems [3-6]. Hence, it finds applications in many household types of equipment like washing machines, air conditioners, refrigerators, mixer, grinders etc. Moreover, BLDC motor is also preferred in industrial equipments like power tools, positioning systems and actuators, electrical vehicles and medical equipments due to above mentioned advantages [3-6]. BLDC motors are electronically commutated motors with three phase distributed windings on the stator and permanent magnets on the rotor [7-10]. It is powered by a DC source via three-phase VSI (Voltage Source Inverter) with switching signals of the switches based on the rotor position as sensed by Hall Effect sensors [10].

A BLDC motor fed by a DBR (Diode Bridge Rectifier) with a high DC link capacitor injects high amount of harmonics at the AC mains. The supply current drawn by such configuration is peaky in nature, having high THD (Total Harmonic Distortion) and results in poor power factor. Many configurations are reported in the literature for the improvement of power quality at AC mains for a single phase and three phase supply [11, 12]. Two stage converters have been in nominal practice which preferably includes a boost stage for PFC and a buck-boost stage for voltage control [13]. Single stage PFC converters are preferred over the multi stage because of requirement of two different controls and high losses in multi stage converters [11, 12].

An IHQRR (Integrated High Quality Rectifier Regulator) combines two converters for attaining an improved power quality at the AC mains [14-18]. The major advantage of single switch in such converters offers high efficiency (reduced
switching losses) and performance similar to a single stage converter. A BIFRED (Boost Integrated Flyback Rectifier Energy Storage DC-DC) converter is an IHQRR which integrates a boost PFC stage with a flyback converter using single switch. The boost converter working in DCM (Discontinuous Conduction Mode) operates as an inherent power factor corrector [11]. The flyback converter is allowed to work in DCM or CCM (Continuous Conduction Mode) depending upon the requirement. A CCM operation requires a current multiplier approach using three sensors (2-voltage and 1-current) whereas a voltage follower approach is used for operation of converter in DCM using single voltage sensor [11, 12].

A requirement in the development of a high performance, low cost BLDC drive encourages the use of BIFRED converter as a front end converter for PFC and voltage control. The cost reduction of the drive is to be considered on account of using minimum number of sensors. Moreover, reducing the switching losses in the VSI to increase the efficiency of the drive is also a major consideration. Finally, the performance of the proposed drive is to be analyzed for speed control with improved power quality at the AC mains.

II. PROPOSED BIFRED CONVERTER FED BLDC MOTOR DRIVE

Fig. 1 shows the proposed IHQRR- BIFRED converter based VSI fed BLDC motor drive using a single voltage sensor. A new approach of controlling the speed of BLDC motor by the DC link voltage control is used [19]. The BIFRED converter is operated in dual DCM to achieve a power factor correction and DC link voltage control by utilizing a voltage follower approach [18]. The integrated boost converter operating in DCM acts as an inherent power factor pre-regulator. Moreover, the flyback converter is also designed to work in DCM for voltage control. A high frequency MOSFET (Metal Oxide Semiconductor Field Effect Transistor) of appropriate rating is used in the front end converter and IGBT’s (Insulated Gate Bipolar Transistor) are used in VSI for low frequency operation. The losses in the VSI are reduced by using a fundamental frequency switching of VSI’s switches to achieve an electronic commutation of the BLDC motor. The proposed drive is designed for a wide range of speed control with improved power quality at the AC mains.

III. OPERATION AND DESIGN OF BIFRED CONVERTER FED BLDC MOTOR DRIVE

An IHQRR-BIFRED converter is designed to operate in a dual DCM. The current in the boost inductor L_i and magnetizing inductance L_m of the HFT (High Frequency Transformer) becomes discontinuous in a switching period. The value of L_i and L_m are to be chosen such that the current in L_i becomes discontinuous before the current in L_m reaches zero for the dual DCM operation as shown in Fig. 2 [18]. The operation of the BIFRED converter is classified into four different modes as shown below [14-18].

**Mode A:** In this mode switch S_w is turned on such that the input current i_L flows through S_w and diode D_b to energize the boost inductor L_i as shown in Fig. 3 (a). The energy stored in blocking capacitor C_b is transferred to the magnetizing inductance of the transformer L_m. Diode D_f remains reversed biased and DC link capacitor C_d supplies the energy to the load which results in reduction of DC link voltage as shown in Fig. 2.

**Mode B:** The switch S_w is turned off in this mode and the current flows through the boost inductor L_i and magnetizing inductance L_m of the HFT, to charge the bulk capacitor C_b as shown in Fig. 3 (b). The energy stored in L_m is transferred to the output side via HFT with diode D_f which is in forward biased position to charge the DC link capacitor C_d, hence the DC link voltage begins to increase in this mode as shown in Fig. 2. At the end of this mode, the inductive energy of the boost inductor is completely discharged and current i_L (or i_m) becomes zero.

**Mode C:** The switch S_w remains in turn off position and the remaining stored energy of the L_m is transferred to the DC link capacitor C_d through HFT as shown in Fig. 3 (c). Hence the voltage across the DC link capacitor C_d increases. In this process the diode D_b remains reverse biased so that current can’t flow through the boost inductor L_i. At the end of this mode the energy stored in magnetizing inductance L_m is completely drained and the bulk capacitor C_b remains at its highest possible voltage.

**Mode D:** In this mode neither of the diodes D_b nor D_f is conducting as shown in Fig. 3 (d). The boost inductor L_i and magnetizing inductance L_m do not have any stored energy. Thus, no transfer of energy through HFT takes place and the required energy to the load is supplied by the DC link capacitor C_d. Hence the voltage across the capacitor starts decreasing as
shown in Fig. 2.

Fig. 2. Waveforms showing different modes in DCM-DCM configuration of BIFRED converter

The design of a BIFRED converter consists of designing and selection of optimal value of boost inductor \( L_i \), turns ratio \( N_1:N_2 \) and magnetizing inductance \( L_m \) of the HFT, bulk capacitor \( C_b \) and DC link capacitor \( C_d \). The EMI filter is also designed to eliminate the ill effect of high switching frequency reflection in the supply system. A BIFRED converter depicts an isolated SEPIC (Single Ended Primary Inductor Converter) but with an extra diode \( D_b \) which allows the boost inductor to work independently in DCM as power factor pre-regulator without disturbing the performance of flyback converter for voltage control. Therefore, the design of BIFRED converter is similar to an isolated SEPIC but with both \( L_i \) and \( L_m \) operating in DCM.

A 500W converter system is designed for controlling the DC link voltage from 40V to 130V for speed control. A single phase supply of 220V (\( \text{Vs} \)), 50Hz (\( f_L \)) is applied to the DBR.

The value of \( V_in \) is expressed and calculated as [13],

\[
V_{in} = \frac{2\sqrt{2}V_s}{\pi} = \frac{2\sqrt{2}\times220}{\pi} = 198V
\]  

(1)

For an isolated SEPIC which is a buck-boost configuration, the DC link voltage \( V_{dc} \) relation with input voltage \( V_{in} \) (voltage across DBR terminals) is given as [12],

\[
V_{dc} = \frac{N_2}{N_1}(1-D)V_{in}
\]  

(2)

Using above equation (2), the duty ratio for the rated DC link voltage (i.e. 130V) is calculated for turn’s ratio \( N_1:N_2=1:2 \) (since desired output voltage is nearly half of the input voltage) as,

\[
D = \frac{\left(\frac{N_2}{N_1}\right)V_{dc}}{V_{in} + \left(\frac{N_2}{N_1}\right)V_{dc}} = \frac{\left(\frac{1}{2}\right)x130}{198 + \left(\frac{1}{2}\right)x130} = 0.2471
\]

The expression for boost inductor \( L_i \) to work in CCM is given as [12],

\[
L_i = \frac{V_{in}D}{f_s\Delta I_{in}}
\]  

(3)

where \( f_s \) is the switching frequency and \( \Delta I_{in} \) is the permitted ripple current in \( L_i \).

At critical conduction mode the current ripple is as,

\[
\Delta I_{in} = 2I_{in}
\]  

(4)

Hence the critical value of inductor to operate at the boundary of CCM and DCM is given and calculated as [12],

\[
L_{ic} = \frac{V_{in}D}{2f_sI_{in}} = \frac{198x0.2471}{2x45000x\frac{500}{198}} = 215.27\mu H
\]  

(5)

Now the value of boost inductor to operate in DCM is evaluated using,

\[
L_i < L_{ic}
\]  

(6)

Hence the value of \( L_i \) is selected using equation (6) as 150\( \mu H \).

The critical value of magnetizing inductance \( L_{mc} \) to operate at the boundary of CCM and DCM is given and calculated as [12],

\[
L_{mc} = \frac{(1-D)^2R_s}{2Df_s\left(\frac{N_2}{N_1}\right)^2} = \frac{(1-0.2471)^2\times130^2}{2Df_s\left(\frac{N_2}{N_1}\right)^2} = 3.446mH
\]

(7)

Hence to operate in a deep DCM, the value of magnetizing inductance \( L_m \) is given as,

\[
L_m << L_{mc}
\]  

(8)

The value of \( L_m \) is taken around 1/10th of the \( L_{mc} \) to guarantee a DCM over wide range of DC link voltage control [20]. The selected value of \( L_m \) using equation (8) is as 350\( \mu H \).

The expression and calculation for bulk capacitor \( C_b \) for \( \Delta V_{ch} \) (permitted ripple voltage in the bulk capacitor) taken as 5\% of peak input voltage is given as is given as [12],
Hence the selected value of bulk capacitor is 750nF.

The value of DC link capacitor $C_d$ for the DC link current $I_{dc}$ and permitted ripple voltage $\Delta V_{dc}$ as 2% of desired DC link voltage $V_{dc}$ is given and calculated as [12],

$$C_d = \frac{I_{dc}}{2\Delta V_{dc}} = \frac{500}{2\times\pi\times50\times0.02\times130} = 2354.36 \mu F$$

(10)

Hence the value of DC link capacitor is selected as 4000 µF (to limit the DC link voltage ripple even less than 2%).

Input LC filter of the PFC converter is designed as given by Vlatkovic et.al. [21]. The maximum value of filter capacitance $C_{max}$ is given and calculated as [21],

$$C_{max} = \frac{I_{peak}}{2\Delta V_{peak}} = \frac{500\sqrt{2}/220}{314\times311} = 574.5nF$$

(11)

where $I_{peak}$ is the peak input current, $V_{peak}$ is the peak input voltage and $\theta$ is the displacement angle.

The value of filter capacitance $C_f$ is selected such that $C_f$ is lower than $C_{max}$, hence the value of $C_f$ is selected as 330nF.

The expression for the calculation of filter inductance $L_f$ is given as [21],

$$L_f = \frac{1}{4\pi^2 f_c^2 C_f} = \frac{1}{4\pi^2 \left(\frac{4500/10}{10^9}\right) \times 330 \times 10^{-9}} = 3.79 mH$$

(12)

where $f_c$ is the cut-off frequency such that $f_c = f_s/10$ [21].

Hence the filter inductance is selected as 4mH.

IV. CONTROL OF BIFRED CONVERTER FED BLDC MOTOR DRIVE

The function of the control unit of BIFRED converter is to generate of PWM (Pulse Width Modulated) signals for the switch $S_w$ to control DC link voltage at the desired value. An inherent power factor correction is achieved since the converter is designed to operate in DCM utilizing a voltage follower approach. The control scheme of the proposed BIFRED converter based VSI fed BLDC motor drive consists of a reference voltage generator, voltage error generator, voltage controller and a PWM generator as shown in Fig. 1.

A. Reference Voltage Generator

A reference DC link voltage $V_{dc*}$ is generated by multiplying the reference speed $N*$ with the motor’s voltage constant $k_v$, as,

$$V_{dc*} = k_v N*$$

(13)

B. Voltage Error Generator

The reference DC link voltage $V_{dc*}$ is compared with the sensed DC link voltage $V_{dc}$ to generate a voltage error signal $V_e$. This voltage error signal is the given to the PI (Proportional-Integral) controller for the necessary control action. The error voltage $V_e$ is given as,

$$V_e = V_{dc*} - V_{dc}$$

(14)

C. Voltage Controller

A voltage PI controller produces a controlled output $V_c$ from the voltage error $V_e$ for the necessary control action. The controller output $V_c$ at any sampling instant $k$ is given as,

$$V_c(k) = V_c(k-1) + K_p \{V_e(k) - V_e(k-1)\} + K_i V_e(k)$$

(15)

where $K_p$ and $K_i$ represent the proportional and integral gains of the voltage PI controller respectively.

D. PWM Generator

A PWM signal is generated by comparing the voltage controller output $V_c$ with a high frequency saw-tooth waveform $m_d(t)$. This PWM signal is given to MOSFET of the BIFRED converter. The switching function is defined as,

$$S_a(t) = \begin{cases} 1 & \text{if } m_d(t) < V_c(t) \\ 0 & \text{else} \end{cases}$$

(16)

where ‘1’ and ‘0’ represent the ‘on’ and ‘off’ condition of the switch respectively.

V. MODELING OF BIFRED CONVERTER FED BLDC MOTOR DRIVE

The modeling of the BLDC motor drive is classified into modeling of the BLDC motor, VSI and the electronic commutation for the operation of BLDC motor. The speed and current derivatives equations of the BLDC motor are obtained to derive its mathematical model. Section “VSI” describes the voltage applied by VSI to the BLDC motor in different switching states. Moreover, the switching sequence of different switches of VSI depending upon the rotor position as sensed by Hall sensors is given in section “Electronic Commutation”. Fig. 4 shows the VSI fed BLDC motor drive.

A. BLDC Motor

For a three phase star connected BLDC motor, per phase voltages ($V_{an}$, $V_{bn}$ and $V_{cn}$) of the BLDC motor is given as [7, 22],
where \( i_a, i_b \) and \( i_c \) are the phase currents, \( e_a, e_b \) and \( e_c \) are the per phase back emf's, \( R_s \) is the per phase resistance, \( L \) and \( M \) is the self and mutual inductance of the stator's winding respectively and \( p \) is the differential operator.

The V-A relation obtained after substituting equation (18) in equation (17) is as,

\[
\begin{bmatrix}
V_a \\
V_b \\
V_c \\
\end{bmatrix} = \begin{bmatrix}
1 & 0 & 0 \\
0 & 1 & 0 \\
0 & 0 & 1
\end{bmatrix}\begin{bmatrix}
i_a \\
i_b \\
i_c
\end{bmatrix} + \begin{bmatrix}
-L-M & 0 & 0 \\
0 & -L-M & 0 \\
0 & 0 & -L-M
\end{bmatrix}\begin{bmatrix}
i_a \\
i_b \\
i_c
\end{bmatrix} + \begin{bmatrix}
e_a \\
e_b \\
e_c
\end{bmatrix}
\]

(19)

Using equation (19), the currents derivative are obtained as,

\[
\begin{bmatrix}
p_i_a \\
p_i_b \\
p_i_c
\end{bmatrix} = \begin{bmatrix}
-L-M & 0 & 0 \\
0 & -L-M & 0 \\
0 & 0 & -L-M
\end{bmatrix}\begin{bmatrix}
i_a \\
i_b \\
i_c
\end{bmatrix} + \begin{bmatrix}
e_a \\
e_b \\
e_c
\end{bmatrix}
\]

(20)

The electromagnetic torque \( T_e \) is given as [7, 22],

\[
T_e = \sum \frac{(e_n - f_n(\theta)\lambda_n)}{\omega_r}
\]

(21)

where \( \omega_r \) represents the rotor speed, \( x \) represent the phase a, b or c and n represents the neutral terminal. This expression faces computational difficulty at zero speed, hence to overcome this, \( e_{sn} \) is defined as [7, 22],

\[
e_{sn} = f_{sn}(\theta)\lambda_{sn}\omega_r
\]

(22)

where \( \lambda_n \) represents the flux and the functions \( f_{sn}(\theta) \) have the same shape as of the back emf. Substituting equation (22) in equation (21),

\[
T_e = \lambda_n \sum f_{sn}(\theta)i_{sn}
\]

(23)

The torque balance equation is given as [7, 22],

\[
T_e - T_l = J \frac{d\omega_r}{dt} + B \omega_r
\]

(24)

where \( T_l \) is load torque, \( J \) is the moment of inertia of the motor and \( B \) is the frictional constant.

Using equation (24), the speed derivative is expressed as,

\[
\begin{aligned}
p_\omega &= \frac{(T_e - T_l - B \omega_r)}{J}
\end{aligned}
\]

(25)

And finally the neutral voltage \( V_{no} \) with respect to point ‘o’ as shown in Fig. 4 is given as [22],

\[
V_{no} = \left( V_{an} + V_{bo} + V_{cn} - (e_{an} + e_{bn} + e_{cn}) \right)/3
\]

(26)

The equations (17)-(26) shown above describes the dynamic model of BLDC motor.

B. Voltage Source Inverter

From Fig. 4, the output voltage of the inverter of phase ‘a’ with respect to potential at point ‘o’ is given as,

\[
V_{ao} = V_{dc}/2 \quad \text{for } S_1=1
\]

(27)

\[
V_{ao} = -V_{dc}/2 \quad \text{for } S_2=1
\]

(28)

\[
V_{ao} = 0 \quad \text{for } S_1=0, S_2=0
\]

(29)

where ‘1’ and ‘0’ represent the ‘on’ and ‘off’ condition of the IGBT’s respectively.

C. Electronic Commutation

The switching sequence of the VSI is the state of switches for a particular rotor position of the BLDC motor as sensed by the Hall Effect position sensor. The turn on and turn off condition of the IGBT’s is represented as ‘1’ or ‘0’ respectively. The switching sequence of VSI for different positions of the rotor is shown in Table-I.

**TABLE I**

<table>
<thead>
<tr>
<th>Hall Signal</th>
<th>Switching Sequence</th>
</tr>
</thead>
<tbody>
<tr>
<td>H_a</td>
<td>S_1, S_2, S_3, S_4, S_5, S_6</td>
</tr>
<tr>
<td>H_b</td>
<td>0, 0, 0, 0, 0, 0, 0, 1</td>
</tr>
<tr>
<td>H_c</td>
<td>60-120, 120-180, 180-240, 240-300, 300-360</td>
</tr>
<tr>
<td>S_1</td>
<td>0, 0, 1, 1, 0, 0, 0, 0, 1</td>
</tr>
<tr>
<td>S_2</td>
<td>0, 1, 0, 0, 1, 0, 0, 0, 0, 1</td>
</tr>
<tr>
<td>S_3</td>
<td>0, 0, 1, 0, 0, 1, 0, 0, 0, 0, 1</td>
</tr>
<tr>
<td>S_4</td>
<td>0, 0, 1, 0, 0, 0, 1, 0, 0, 0, 1</td>
</tr>
<tr>
<td>S_5</td>
<td>0, 0, 1, 0, 0, 0, 0, 1, 0, 0, 1</td>
</tr>
<tr>
<td>S_6</td>
<td>0, 0, 1, 0, 0, 0, 0, 0, 1, 0, 0</td>
</tr>
</tbody>
</table>

VI. PERFORMANCE EVALUATION

The performance of the proposed drive system is evaluated on the basis of various mechanical and electrical parameters of the BLDC motor and the front end BIFRED converter. Speed (N), electromagnetic torque (\( T_e \)) and stator current (\( i_s \)) of the BLDC motor are estimated for determining the performance of
the BLDC motor. Whereas, electrical parameters such as DC link voltage ($V_{dc}$), boost inductor current ($i_{Li}$), magnetizing current of HFT ($i_{Lm}$) and voltage across bulk capacitor ($v_{Cb}$) are shown for satisfactory performance of BIFRED converter. Moreover, the supply voltage ($v_s$) and supply current ($i_s$) determine the performance in terms of power quality of the drive. Parameters such as THD (Total Harmonic Distortion), DPF (Displacement Power Factor), PF (Power Factor) and CF (Crest Factor) of the supply current are used for the power quality assessment. Switch voltage ($v_{sw}$) and switch current ($i_{sw}$) are also determined for deciding the rating of MOSFET to be used for designing a BIFRED converter.

Fig. 5 shows the performance of the proposed drive at rated DC link voltage and rated load. The supply current obtained is sinusoidal and in phase with the supply voltage. The current $i_{Li}$ and $i_{Lm}$ are discontinuous as shown in Fig. 5, thus verifying the dual DCM operation of the BIFRED converter. The switch peak voltage and peak current are around 700V and 22A respectively, which are quite acceptable for designing a 500W system. Table-II shows the performance of proposed drive under speed control from 30V to 130V. The THD of supply current is found below 5% and power factor above 0.99 over complete range of speed control which is under the acceptable limits by IEC 61000-3-2.

Table-II

<table>
<thead>
<tr>
<th>$V_{dc}$ (V)</th>
<th>Speed (rpm)</th>
<th>THD of $I_s$ (%)</th>
<th>DPF</th>
<th>PF</th>
<th>$I_s$ (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>30</td>
<td>230</td>
<td>3.28</td>
<td>0.9977</td>
<td>0.9972</td>
<td>1.006</td>
</tr>
<tr>
<td>40</td>
<td>460</td>
<td>3.08</td>
<td>0.9986</td>
<td>0.9981</td>
<td>1.222</td>
</tr>
<tr>
<td>50</td>
<td>690</td>
<td>2.86</td>
<td>0.9991</td>
<td>0.9987</td>
<td>1.431</td>
</tr>
<tr>
<td>60</td>
<td>910</td>
<td>2.62</td>
<td>0.9995</td>
<td>0.9992</td>
<td>1.635</td>
</tr>
<tr>
<td>70</td>
<td>1125</td>
<td>2.29</td>
<td>0.9997</td>
<td>0.9994</td>
<td>1.839</td>
</tr>
<tr>
<td>80</td>
<td>1340</td>
<td>1.84</td>
<td>0.9998</td>
<td>0.9996</td>
<td>2.046</td>
</tr>
<tr>
<td>90</td>
<td>1550</td>
<td>1.49</td>
<td>0.9998</td>
<td>0.9998</td>
<td>2.262</td>
</tr>
<tr>
<td>100</td>
<td>1770</td>
<td>1.38</td>
<td>1.0000</td>
<td>0.9999</td>
<td>2.485</td>
</tr>
<tr>
<td>110</td>
<td>1980</td>
<td>1.30</td>
<td>1.0000</td>
<td>0.9999</td>
<td>2.715</td>
</tr>
<tr>
<td>120</td>
<td>2190</td>
<td>1.27</td>
<td>1.0000</td>
<td>0.9999</td>
<td>2.95</td>
</tr>
<tr>
<td>130</td>
<td>2420</td>
<td>1.25</td>
<td>0.9999</td>
<td>0.9998</td>
<td>3.236</td>
</tr>
</tbody>
</table>

Performance of the proposed drive system is also evaluated for dynamic conditions. Fig. 6 shows the performance during start-up and speed control which is obtained quite satisfactory with smooth control. Fig. 7 shows the supply current and its harmonic spectrum at rated voltage and rated loading condition. The performance of drive is also evaluated for varying supply voltage from 170V-270V to demonstrate the satisfactory performance at the practical situations and is tabulated in Table-III.

Switch peak voltage ($v_{sw}$), switch peak current ($i_{peak}$) and switch rms current ($i_{rms}$) are tabulated in Table-IV for different loading on the BLDC motor. Peak voltage and peak current on the switch are used for determining the rating of the switch and rms current flowing through the switch which decides the
thermal rating of the heat sink to be designed. Fig. 8 shows the variation of THD of supply current and power factor with DC link voltage (Fig. 8 (a)) and supply voltage (Fig. 8 (b)) respectively. The characteristics obtained show that the power quality indices are obtained within the recommended limits by IEC 61000-3-2, thus an improved power quality is achieved for a wide range of speed control and supply voltage variation.

<p>| TABLE III |
| POWER QUALITY PARAMETERS OF PROPOSED SYSTEM WITH INPUT AC VOLTAGE VARIATION |</p>
<table>
<thead>
<tr>
<th>( V_s ) (V)</th>
<th>THD of ( I_s ) (%)</th>
<th>DPF</th>
<th>PF</th>
<th>( I_s ) (A)</th>
<th>CF</th>
</tr>
</thead>
<tbody>
<tr>
<td>170</td>
<td>0.82</td>
<td>0.9982</td>
<td>0.9982</td>
<td>4.12</td>
<td>1.414</td>
</tr>
<tr>
<td>180</td>
<td>0.88</td>
<td>0.9992</td>
<td>0.9992</td>
<td>3.912</td>
<td>1.414</td>
</tr>
<tr>
<td>190</td>
<td>0.97</td>
<td>0.9995</td>
<td>0.9995</td>
<td>3.7</td>
<td>1.414</td>
</tr>
<tr>
<td>200</td>
<td>0.99</td>
<td>0.9997</td>
<td>0.9997</td>
<td>3.509</td>
<td>1.414</td>
</tr>
<tr>
<td>210</td>
<td>1.14</td>
<td>0.9999</td>
<td>0.9998</td>
<td>3.339</td>
<td>1.414</td>
</tr>
<tr>
<td>220</td>
<td>1.25</td>
<td>0.9999</td>
<td>0.9998</td>
<td>3.236</td>
<td>1.414</td>
</tr>
<tr>
<td>230</td>
<td>1.27</td>
<td>1</td>
<td>0.9999</td>
<td>3.046</td>
<td>1.414</td>
</tr>
<tr>
<td>240</td>
<td>1.28</td>
<td>1</td>
<td>0.9999</td>
<td>2.916</td>
<td>1.414</td>
</tr>
<tr>
<td>250</td>
<td>1.4</td>
<td>1</td>
<td>0.9999</td>
<td>2.8</td>
<td>1.414</td>
</tr>
<tr>
<td>260</td>
<td>1.45</td>
<td>0.9999</td>
<td>0.9998</td>
<td>2.689</td>
<td>1.414</td>
</tr>
<tr>
<td>270</td>
<td>1.58</td>
<td>0.9998</td>
<td>0.9997</td>
<td>2.59</td>
<td>1.414</td>
</tr>
</tbody>
</table>

<p>| TABLE IV |
| VOLTAGE AND CURRENT STRESS ON SWITCH ON DIFFERENT LOADING CONDITION |</p>
<table>
<thead>
<tr>
<th>Load</th>
<th>( V_p )</th>
<th>( I_p )</th>
<th>( I_{\text{rms}} ) (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>680</td>
<td>13</td>
<td>0.48</td>
</tr>
<tr>
<td>20</td>
<td>680</td>
<td>14</td>
<td>0.54</td>
</tr>
<tr>
<td>30</td>
<td>680</td>
<td>15</td>
<td>0.62</td>
</tr>
<tr>
<td>40</td>
<td>690</td>
<td>16</td>
<td>0.76</td>
</tr>
<tr>
<td>50</td>
<td>690</td>
<td>17</td>
<td>0.812</td>
</tr>
<tr>
<td>60</td>
<td>690</td>
<td>18</td>
<td>0.919</td>
</tr>
<tr>
<td>70</td>
<td>690</td>
<td>19</td>
<td>1.06</td>
</tr>
<tr>
<td>80</td>
<td>700</td>
<td>20</td>
<td>1.14</td>
</tr>
<tr>
<td>90</td>
<td>700</td>
<td>21</td>
<td>1.27</td>
</tr>
<tr>
<td>100</td>
<td>700</td>
<td>22</td>
<td>1.485</td>
</tr>
</tbody>
</table>

VII. CONCLUSION

A BIFRED converter of an IHQRR family has been used for improved power quality operation of BLDC motor drive. A BIFRED converter fed VSI based BLDC motor drive has been proposed for speed control using a single voltage sensor. A BIFRED converter operating in dual DCM has been utilized as a front end converter for the power factor correction and DC link voltage control. Electronic commutation of the BLDC motor which utilizes a fundamental frequency switching of the VSI has been used for obtaining reduced switching losses in the VSI. An improved power quality operation for a wide range of speed control has been obtained under the recommended limits by international power quality standard such as IEC 61000-3-2. A satisfactory performance of the drive has also been obtained for varying supply voltage to demonstrate the behavior in practical situation. Moreover, switch stress has also been analyzed for deciding the switch rating and size of heat sink. The proposed converter topology has been found suitable for the design of high performance BLDC motor drive with improved power quality at the AC mains.

APPENDIX

BLDC Motor Rating: 4 pole, \( P_{\text{rated}} \) (Rated Power) = 0.5 HP (377 W), \( V_{\text{rated}} \) (Rated DC link Voltage) = 130 V, \( T_{\text{rated}} \) (Rated Torque) = 1.2 Nm, \( \omega_{\text{rated}} \) (Rated Speed) = 3000 rpm, \( K_b \) (Back
EMF Constant) = 34 V/krpm, $K_t$ (Torque Constant) = 0.32 Nm/A, $R_{ph}$ (Phase Resistance) = 2.68 $\Omega$, $L_{ph}$ (Phase Inductance) = 5.31 mH, $J$ (Moment of Inertia) = 1.3 kg-cm².

REFERENCES


Bhim Singh received his B.E. in Electrical Engineering from the University of Roorkee, Roorkee, India, in 1977 and his M.Tech. and Ph.D. from the Indian Institute of Technology (IIT) Delhi, New Delhi, India, in 1979 and 1983, respectively. In 1983, he joined Department of Electrical Engineering, University of Roorkee, as a Lecturer, and in 1988 he became a Reader. In December 1990, he joined Department of Electrical Engineering, IIT Delhi, as an Assistant Professor. He became an Associate Professor in 1994 and a Professor in 1997. He has guided 39 Ph.D. dissertations, 120 M.E./M.Tech./M.S.(R) theses, and 60 BE/B.Tech. Projects. His areas of interest include power electronics, electrical machines and drives, renewable energy systems, active filters, FACTS, HVDC and power quality.

Dr. Singh is a Fellow of the Indian National Academy of Engineering (INAIE), the National Science Academy (NSc), the Institute of Electrical and Electronics Engineers (IEEE), the Institute of Engineering and Technology (IET), the Institution of Engineers (India) (IE(I)), and the Institution of Electronics and Telecommunication Engineers (IETE). He is also a life member of the Indian Society for Technical Education (ISTE), the System Society of India (SSI), and the National Institution of Quality and Reliability (NIQR).

Vashist Bist received his Diploma and B.E. in Instrumentation and Control Engineering from Sant Longowal Institute of Engineering and Technology (SLIET), Longowal, Sangrur, Punjab, India in 2007 and 2010 respectively. He is currently doing PhD. in Department of Electrical Engineering, Indian Institute of Technology Delhi (IIT Delhi). His areas of interests include power electronics, electrical machines and drives.