Nonisolated Bidirectional Soft Switching SEPIC/ZETA Converter with Reduced Ripple Currents

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Abstract

A novel nonisolated bidirectional soft switching SEPIC/ZETA converter having reduced ripple currents has been proposed and characterized in the present paper. Based on the original bidirectional SEPIC/ZETA components, auxiliary two switches and an inductor are added to form a new direct power delivery path between input and output. Proposed converter can be operated in forward SEPIC and reverse ZETA modes with reduced ripple currents and higher voltage gains owing to the optimized selection of duty ratios. All switches in the proposed converter can be operated at zero-current-switching (ZCS) turn-on and/or turn-off by soft current commutation among them. Therefore, switching and conduction losses of the proposed converter have also been considerably reduced compared to the conventional bidirectional SEPIC/ZETA converter. Operation principles and characteristics of the proposed converter are analyzed in detail, and verified with some simulation and experimental results.

Key words: Bidirectional SEPIC/ZETA converter, ripple current, soft current commutation, soft switching

I. INTRODUCTION

Bidirectional dc-dc converter can manipulate bilateral power flow between two dc sources only using a single circuit structure. Therefore, the weight, volume, and cost of the overall system can be reduced with simplified circuit composition [1]. Owing to such good features, bidirectional dc-dc converters have been increasingly used in battery charger/discharger, fuel cell hybrid power system, dc uninterruptible power supply, and energy regenerative system in automotive applications [2]–[9].

When galvanic isolation is not needed, nonisolated converters are preferred due to their simplicity and higher efficiency than isolated converters. Several nonisolated bidirectional dc-dc converters have been reported in literatures; bidirectional boost/buck-derived converters [10]–[13], Cuk [14], SEPIC/ZETA [15], multilevel converter [16], [17], and coupled inductor type converters [18], [19]. Among them, multiphase interleaved converters are often adopted to reduce the voltage ripple and filter size by reducing ripple components of the inductor current [20]–[22]. They can enhance the performance of the circuit; however, the complexity of overall circuit system can be increased. Control reliability might be also deteriorated with increased interleaving phases.

Without any interleaved techniques, unidirectional SEPIC and ZETA converters featuring reduced ripple currents have been proposed in [23], [24]. As shown in Fig. 1, they consist of the original SEPIC or ZETA components plus auxiliary diode and switch to form a new direct power delivery path between input and output. By shortening duration time for original SEPIC or ZETA operation and expanding duration time for direct power link operation, inductor ripple currents and switching voltages of main switch and diode can be reduced. However, they still have hard switching properties. Especially, diodes suffer from severe reverse recovery problem.

In order to overcome these hard switching problems, a new nonisolated bidirectional soft switching SEPIC/ZETA converter with reduced ripple currents is proposed in this paper. Based on the modified SEPIC topology in Fig. 1 (a), just a small inductor is added on the auxiliary power delivery path and diodes are replaced by active switches for bidirectional power flow control. Using a single circuit structure, SEPIC and ZETA operations are implemented in forward and reverse directions, respectively. Both step-up and step-down operations are available regardless of power conversion directions like the original bidirectional SEPIC/ZETA converter. Owing to the duality between SEPIC and ZETA converters, almost same
II. OPERATION ANALYSIS OF THE PROPOSED CONVERTER

A. Circuit Structure

The proposed converter can be divided into two parts as shown in Fig. 2. The first part is the original nonisolated bidirectional SEPIC/ZETA converter consisting of inductors \( L_1 \) and \( L_2 \); capacitors \( C_{in}, C_s, \) and \( C_o \); switches \( S_1 \) and \( S_2 \). The second part is an additional circuit consisting of switches \( S_3 \) and \( S_4 \), and an inductor \( L_a \). The additional circuit provides a new direct power delivery path between input and output. SEPIC and ZETA operations are implemented in forward and reverse directions, respectively.

In SEPIC operation, \( S_1 \) acts for main switch; \( S_2 \) for synchronous rectifier; \( S_3 \) and \( S_4 \) for auxiliary switches. In ZETA operation, \( S_1 \) conducts for synchronous rectifier; \( S_2 \) for main switch; \( S_3 \) and \( S_4 \) for auxiliary switches. \( L_a \) induces the soft current transition between switches.

B. Mode Analysis

In the proposed converter, \( L_a \) is much smaller than \( L_1 \) and \( L_2 \). Therefore, following basic operation analysis ignores the effect of \( L_a \) and treats the proposed converter as conventional hard switching converter to simplify the analysis. During each switching cycle, the proposed converter has three distinct operation modes in SEPIC and ZETA operations, respectively. Operation waveforms for forward SEPIC mode are shown in Fig. 3.

**Mode 1 \([t_0-t_1]\):** From \( t_0 \) to \( t_1 \), only \( S_1 \) conducts while the other switches idle. Average inductor voltage is zero at steady state, so the voltage of \( C_s \) equals to input voltage \( V_{in} \) [26]. Voltages across \( L_1 (v_{i1}) \) and \( L_2 (v_{i2}) \) are both equal to \( V_{in} \). Currents through \( L_1 (i_{i1}) \) and \( L_2 (i_{i2}) \) increase with slopes of \( V_{in}/L_1 \) and \( V_{in}/L_2 \), respectively. The current flowing through \( S_1 \) \((i_{s1})\) is sum of \( i_{i1} \) and \( i_{i2} \). The drain-source voltages of \( S_1 \) \((v_{s1})\) and \( S_2 \) \((v_{s2})\) are 0V and \( V_{in}+V_o \), respectively, where \( V_o \) is output voltage. At the beginning of this mode, capacitor charging current flows from \( V_i \) terminal to \( S_1 \) through output capacitor of \( S_1 \) and the body diode of \( S_1 \). Therefore, the drain-source voltages of \( S_1 \) \((v_{s1})\) and \( S_4 \) \((v_{s4})\) become \( V_o \) and 0V, respectively. In fact, \( S_1 \) should be turned off after \( t_0 \) to satisfy the continuity of inductor currents.

**Mode 2 \([t_1-t_2]\):** From \( t_1 \) to \( t_2 \), only \( S_2 \) conducts, and the other switches idle. The source voltage of \( S_2 \) is \( V_o \), so \( v_{i1} \) and \( v_{i2} \) are both \(-V_o\). \( i_{i1} \) and \( i_{i2} \) decrease with slopes of \(-V_o/L_1\) and \(-V_o/L_2\), respectively. The current through \( S_2 \) \((i_{s2})\) is sum of \( i_{i1} \) and \( i_{i2} \). At the beginning of this mode, voltage difference between drain voltage of \( S_1 (V_{in}+V_o) \) and \( V_o \) terminal induces capacitor charging current flowing through auxiliary current path. Assuming the same output capacitances of \( S_1 \) and \( S_4 \), that voltage difference equally charges output capacitor of \( S_1 \) and \( S_4 \) by \( V_o/2 \), respectively. Simultaneously, \( v_{s3} \) and \( v_{s4} \) in step-up operation becomes \((-V_{in}+V_o)/2\) and \((V_{in}+V_o)/2\), respectively. In step-down operation, they are
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Fig. 3. SEPIC operation waveforms of the proposed converter in (a) step-up and (b) step-down.

0V and $V_{in}$, respectively. $S_2$ can be turned on after $t_1$ and turned off before $t_2$, so synchronous rectification and ZVS can be achieved.

Mode 3 $[t_{2} - t_{0}']$: Between $t_2$ and $t_0'$, $S_3$ and $S_4$ conduct, and $S_1$ and $S_2$ do not conduct. This mode is added to conventional SEPIC/ZETA converter to provide additional power deliver path between input and output, thus enhancing the performance of the proposed converter. As $v_{S1}$ is $V_o$, $v_{S2}$ becomes $V_{in}$. Therefore, both $v_{L1}$ and $v_{L2}$ are $(V_{in} - V_o)/L_1$ and $(V_{in} - V_o)/L_2$, respectively. Those slope change values of inductors are much smaller than those of previous modes. Consequently, ripple currents of inductors can be considerably reduced. The current through $S_3$ and $S_4 (i_{La})$ is sum of $i_{L1}$ and $i_{L2}$. Therefore, $i_{L1}$ and $i_{L2}$ have positive slopes during step-up operation, while positive slopes during step-down operation. $S_1$ should be turned off before $t_0'$ to prevent the reverse short current from $V_o$ terminal to ground through auxiliary current path and $S_1$.

Reverse ZETA operation waveforms are shown in Fig. 4.

Fig. 4. ZETA operation waveforms of the proposed converter in (a) step-up and (b) step-down.

Negative polarity of $i_{L1}$ and $i_{L2}$ means for reverse power flow in ZETA operation. The principle of ZETA operation of the proposed converter is almost similar to that of SEPIC operation due to duality between SEPIC and ZETA converters. Therefore, the specific analysis for ZETA operation is skipped in this paper.

C. Conversion Ratio

Using the voltage-time balance principle, and assuming the 100% power conversion efficiency, the voltage and current conversion ratios of the proposed converter can be determined by:

$$M = \frac{V_o}{V_{in}} = \frac{I_{in}}{I_o} = \frac{T - t_{S2}}{T - t_{S1}} = 1 - d_2 \frac{1 - d_2}{1 - d_1}$$

(1)

Here, $I_{in}$ and $I_o$ refer to input and output currents, respectively. $t_{S1}$ and $t_{S2}$ correspond to the duration times of $S_1$ and $S_2$, respectively. Switching duty ratios $d_1$ and $d_2$ are given by $d_1 = t_{S1}/T$ and $d_2 = t_{S2}/T$, where $T$ is repeated switching period. $d_1$ must be larger than $d_2$ to step up output voltage and vice versa.
As $d_1$ and $d_2$ become smaller, the power conversion efficiency of the proposed converter increases because the low ripple current effect of Mode 3 can be maximized with considerably reduced overall circulation currents. As a result, conduction and switching losses of switches and dc resistive losses of inductors and capacitors can be reduced.

### III. DESIGN PARAMETERS

Some useful design parameters are presented in this section. Here, $L_a$ is ignored to simplify the design. To maximize the ripple reduction effect of the proposed converter, $d_1$ and $d_2$ should be minimized and $d_3$ needs to be maximized. Here, $d_3$ (=1−$d_1$−$d_2$) denotes duty ratio of $S_3$ and $S_4$. In SEPIC operation, therefore, duty ratios can be determined as:

\[
\begin{align*}
\text{step-up: } & \quad d_1 = 1 - (1 - d_2)/M \ (d_2: \text{minimum}) \\
\text{step-down: } & \quad d_2 = 1 - (1 - d_1)/M \ (d_1: \text{minimum})
\end{align*}
\]

(2)

In ZETA operation, likewise, duty ratios are determined by:

\[
\begin{align*}
\text{step-up: } & \quad d_1 = 1 - (1 - d_1)/M \ (d_1: \text{minimum}) \\
\text{step-down: } & \quad d_2 = 1 - (1 - d_2)/M \ (d_2: \text{minimum})
\end{align*}
\]

(3)

where $M$ is voltage conversion ratio defined in (1).

For the proposed converter, inductor ripple current becomes maximum value between $V_{in} d_1 T/L$ and $V_{in} d_2 T/L$, where $L$ is $L_1$ or $L_2$. This formula can be also applied to conventional SEPIC converter; however, ripple value in the proposed converter is much smaller than conventional SEPIC converter owing to the reduction of $d_1$ and $d_2$. Inflection points of inductor currents such as $i_{L1}(t_0)$, $i_{L1}(t_1)$, $i_{L1}(t_2)$, $i_{L2}(t_1)$, $i_{L2}(t_2)$, and $i_{L2}(t_2)$ (Fig. 3) are defined as $I_1$, $I_2$, $I_3$, $I_4$, $I_5$, and $I_6$, respectively. They are related to each other as follows:

\[
\begin{align*}
I_1 &= i_{L1}(t_0) \\
I_2 &= i_{L1}(t_1) = I_1 + \frac{V_{in} d_1 T}{L_1} \\
I_3 &= i_{L1}(t_2) = I_1 + \frac{V_{in} d_1 T - V_o d_2 T}{L_1} \\
I_4 &= i_{L2}(t_0) \\
I_5 &= i_{L2}(t_1) = I_4 + \frac{V_o d_1 T}{L_2} \\
I_6 &= i_{L2}(t_2) = I_4 + \frac{V_o d_1 T - V_o d_2 T}{L_2}
\end{align*}
\]

(4)

Average of $i_{L1}$ equals to $I_0$ as:

\[
I_{in} = i_{L1,avg} = \frac{1}{2} \left( (I_1 + I_2) \cdot d_1 + (I_2 + I_3) \cdot d_2 + (I_3 + I_4) \cdot d_3 \right)
\]

(5)

Substituting (4) into (6) and using (1), $I_1$ is obtained by:

\[
I_1 = I_{in} - (d_1 - d_2 d_3) \cdot \frac{V_{in} T}{4 L_1}
\]

(6)

Charge balance of $C_s$ states as follows:

\[
-(I_4 + I_5) \cdot d_1 + (I_2 + I_3) \cdot d_2 - (I_6 + I_4) \cdot d_3 = 0
\]

(7)

Substituting (4) and (5) into (8), and using (1) and (7), $I_4$ is obtained by:

\[
I_4 = \frac{d_2}{1 - d_2} I_{in} + \frac{d_1 d_2 d_3}{1 - d_1} \frac{V_{in} T}{2 L_1} - \frac{d_1 d_2 d_3 - d_3 d_4}{1 - d_1} \frac{V_{in} T}{2 L_2}
\]

(9)

All other inflection values in (4) and (5) can be exactly determined using (7) and (9). For the ZETA operation, the same method as above can be also applied to derive inflection points of inductor currents. Knowing these values, other design parameters such as inductor average currents, switch peak and root-mean-square (rms) currents, capacitor ripple voltages and rms currents can be obtained by simple algebra. Typical capacitor currents of the proposed converter in step-up mode are shown in Fig. 5. Here, $i_{Cin}$, $i_{Co}$, and $i_{Cs}$ are currents of $C_{in}$, $C_o$, and $C_s$, respectively. For the capacitor ripple voltage calculation, capacitor charge can be achieved from local maximum area enclosed by capacitor current and time axis, and then it is divided into its capacitance such as $C_{in}$, $C_o$, or $C_s$.

According to the operating conditions, capacitor ripple voltages can have several different values. Several major design parameters of the proposed converter are summarized in Table I. The detailed derivations are skipped to save the space of this paper.

### IV. ACTUAL CONVERSION RATIO AND EFFICIENCY CONSIDERING RESISTIVE LOSSES

An equivalent circuit for the proposed converter containing resistive elements of inductors and switches is shown in Fig. 6. $r_{L1}$ and $r_{L2}$ represent the equivalent series resistance of $L_1$ and $L_2$, respectively. $r_{S1}$, $r_{S2}$, $r_{S3}$, and $r_{S4}$ mean the on-state drain-source resistance of $S_1$, $S_2$, $S_3$, and $S_4$, respectively. Including these resistive loss elements, conversion ratio and efficiency can be determined using the methodology in [27].
### TABLE I
Several design parameters of the proposed converter.

<table>
<thead>
<tr>
<th>Conversion ratio</th>
<th>SEPIC mode</th>
<th>ZETA mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>( M = \frac{V_o}{V_{in}} = 1 - \frac{d_2}{d_1} )</td>
<td>( \frac{V_o}{V_{in}} = 1 - \frac{d_2}{d_1} )</td>
<td>( \frac{V_o}{V_{in}} = 1 - \frac{d_2}{d_1} )</td>
</tr>
<tr>
<td>Duty ratio selection</td>
<td>( d_2 = 1 - (1 - d_2)/M ) (where, ( d_2 ) is minimum)</td>
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<tr>
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<td></td>
</tr>
<tr>
<td>Inductor ripple current</td>
<td>( A_i = \max \left( \frac{V_o d_2 T}{I_i} , \frac{V_o d_1 T}{I_i} \right) )</td>
<td>( A_i = \max \left( \frac{V_o d_2 T}{I_i} , \frac{V_o d_1 T}{I_i} \right) )</td>
</tr>
<tr>
<td>Induction points of inductor currents</td>
<td>( I_i - I_o(t_1) = \frac{V_o}{2L_i} )</td>
<td>( I_i - I_o(t_1) = \frac{V_o}{2L_i} )</td>
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<tr>
<td>( I_i - I_o(t_2) = \frac{V_o}{2L_i} )</td>
<td>( I_i - I_o(t_2) = \frac{V_o}{2L_i} )</td>
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<tr>
<td>( I_i - I_o(t_3) = \frac{V_o}{2L_i} )</td>
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<tr>
<td>( I_i = I_o(t_4) = \frac{V_o}{2L_i} )</td>
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<tr>
<td>( I_i = I_o(t_5) = \frac{V_o}{2L_i} )</td>
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<tr>
<td>( I_i = I_o(t_7) = \frac{V_o}{2L_i} )</td>
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<td></td>
</tr>
<tr>
<td>Inductor average currents</td>
<td>( \frac{d_1}{2} \left( I_i + I_o(t_3) \right) + \frac{d_2}{2} \left( I_i + I_o(t_4) \right) )</td>
<td>( \frac{d_1}{2} \left( I_i + I_o(t_3) \right) + \frac{d_2}{2} \left( I_i + I_o(t_4) \right) )</td>
</tr>
<tr>
<td>Switch peak currents</td>
<td>( I_{p1,sep} = I_{p1,zet} = I_1 + I_2 )</td>
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<tr>
<td>Switch peak voltages</td>
<td>( V_{p1,sep} = V_{p1,zet} = V_o )</td>
<td>( V_{p1,sep} = V_{p1,zet} = V_o )</td>
</tr>
<tr>
<td>( \frac{d_1}{3} \left( I_i + I_o(t_3) \right)^2 + \frac{d_2}{3} \left( I_i + I_o(t_4) \right)^2 )</td>
<td>( \frac{d_1}{3} \left( I_i + I_o(t_3) \right)^2 + \frac{d_2}{3} \left( I_i + I_o(t_4) \right)^2 )</td>
<td></td>
</tr>
<tr>
<td>Switch rms currents</td>
<td>( I_{r1,sep} = \frac{d_1}{2} \left( I_i + I_o(t_3) \right)^2 + \frac{d_2}{2} \left( I_i + I_o(t_4) \right)^2 )</td>
<td>( I_{r1,sep} = \frac{d_1}{2} \left( I_i + I_o(t_3) \right)^2 + \frac{d_2}{2} \left( I_i + I_o(t_4) \right)^2 )</td>
</tr>
<tr>
<td>Capacitor ripple voltages</td>
<td>( \Delta V_c = \frac{1}{C_i} \left( \frac{V_o d_2 T}{d_1 I_i} \right)^2 )</td>
<td>( \Delta V_c = \frac{1}{C_i} \left( \frac{V_o d_2 T}{d_1 I_i} \right)^2 )</td>
</tr>
<tr>
<td>Capacitor rms currents</td>
<td>( I_{c1,sep} = \frac{1}{d_1} \left( \frac{V_o d_2 T}{d_1 I_i} \right)^2 )</td>
<td>( I_{c1,sep} = \frac{1}{d_1} \left( \frac{V_o d_2 T}{d_1 I_i} \right)^2 )</td>
</tr>
</tbody>
</table>

\( I_{p1,sep} = I_{p1,zet} = I_1 + I_2 \) (approximation) \( < i_2 > i_1 \) and \( \frac{d_2}{2} \left( I_i + I_o(t_4) \right) \) (real) \( < i_2 > i_1 \)

\( I_{r1,sep} = \frac{d_1}{2} \left( I_i + I_o(t_3) \right)^2 + \frac{d_2}{2} \left( I_i + I_o(t_4) \right)^2 \) \( < i_2 > i_1 \)

\( I_{c1,sep} = \frac{1}{d_1} \left( \frac{V_o d_2 T}{d_1 I_i} \right)^2 \) \( < i_2 > i_1 \)
Conversion ratio and efficiency for forward SEPIC operation of the proposed converter can be derived as follows. Because average inductor voltage is zero, the average voltage of $C_s$ ($V_{Cs}$) is obtained by:
\[ V_{Cs} = V_{in} - I_{L1} \cdot r_{L1} + I_{L2} \cdot r_{L2} \] (10)
Here, $I_{L1}$ and $I_{L2}$ are average values of $i_{L1}$ and $i_{L2}$ over one switching period, respectively, at steady state. When $S_1$ is turned on and the others are turned off, average values of $v_{L1}$, $v_{L2}$, $i_{Co}$, and $i_{Cs}$ are given by:
\[ V_{L1}^{d1} = V_{L2}^{d1} = -V_o - I_{L2} \cdot r_{L2} - (I_{L1} + I_{L2}) \cdot r_{S1} \] (11)
\[ I_{Co}^{d1} = \frac{V_o}{R} \] (12)
\[ I_{Cs}^{d1} = -I_{L2} \] (13)
Here, $R$ denotes load resistance. When $S_2$ is turned on and the others are turned off, average values of $v_{L1}$, $v_{L2}$, $i_{Co}$, and $i_{Cs}$ are obtained as:
\[ V_{L1}^{d2} = V_{L2}^{d2} = V_{in} - I_{L1} \cdot r_{L1} - (I_{L1} + I_{L2}) \cdot r_{S2} \] (14)
\[ I_{Co}^{d2} = I_{L1} + I_{L2} - \frac{V_o}{R} \] (15)
\[ I_{Cs}^{d2} = I_{L1} \] (16)
When $S_3$ and $S_4$ are turned on and the others are idle, average values of $v_{L1}$, $v_{L2}$, $i_{Co}$, and $i_{Cs}$ are given as:
\[ V_{L1}^{d3} = V_{L2}^{d3} = -V_o - I_{L2} \cdot r_{L2} - (I_{L1} + I_{L2}) \cdot r_{S3} \] (17)
\[ I_{Co}^{d3} = I_{L1} + I_{L2} - \frac{V_o}{R} \] (18)
\[ I_{Cs}^{d3} = -I_{L2} \] (19)
By applying ampere-time balance on $C_o$ and $C_s$, following equations are obtained as:
\[ I_{Co}^{d1} \cdot d_1 + I_{Co}^{d2} \cdot d_2 + I_{Co}^{d3} \cdot d_3 = 0 \] (20)
\[ I_{Cs}^{d1} \cdot d_1 + I_{Cs}^{d2} \cdot d_2 + I_{Cs}^{d3} \cdot d_3 = 0 \] (21)
Substituting (12), (15), and (18) into (20), $I_{L1} + I_{L2}$ is given by:
\[ I_{L1} + I_{L2} = \frac{V_o}{R} \cdot \frac{1}{1-d_1} \] (22)
Substituting (13), (16), and (19) into (21), $I_{L2}$ is related with $I_{L1}$ as follows:
\[ I_{L2} = I_{L1} \cdot \frac{d_2}{1-d_2} \] (23)
Substituting (23) into (22), $I_{L1}$ and $I_{L2}$ are obtained as:
\[ I_{L1} = I_{in} = \frac{V_o}{R} \cdot \frac{1-d_2}{1-d_1} \] (24)
\[ I_{L2} = \frac{V_o}{R} \cdot \frac{d_2}{1-d_1} \] (25)

By using the voltage-time balance principle on $L_1$,
\[ V_{L1}^{d1} \cdot d_1 + V_{L1}^{d2} \cdot d_2 + V_{L1}^{d3} \cdot d_3 = 0 \] (26)
By substituting (11), (14), (17), (24), and (25) into (26), actual voltage gain for ZETA operation is achieved by:
\[ \frac{V_o}{V_{in}} = \frac{1-d_2}{1-d_1} \]
\[ \frac{R(1-d_2)^2}{R(1-d_1)^2 + r_{L1}(1-d_1)^2 + r_{L2}d_2^2 + r_{S4}d_1 + r_{S2}d_2 + (r_{S3} + r_{S4})} \cdot d_3 \] (27)
Efficiency is obtained by:
\[ \eta = \frac{P_o}{P_{in}} = \frac{V_o^2}{V_{in}I_{in}} = \frac{R(1-d_1)^2}{R(1-d_1)^2 + r_{L1}(1-d_1)^2 + r_{L2}d_2^2 + r_{S4}d_1 + r_{S2}d_2 + (r_{S3} + r_{S4})} \cdot d_3 \] (28)

Conversion ratio and efficiency for reverse ZETA operation of the proposed converter can be also derived using the similar procedure as above. Here, the results are summarized. Actual voltage gain for ZETA operation is
\[ \frac{V_o}{V_{in}} = \frac{1-d_1}{1-d_2} \]
\[ \frac{R(1-d_2)^2}{R(1-d_2)^2 + r_{L1}(1-d_2)^2 + r_{L2}d_2^2 + r_{S4}d_1 + r_{S2}d_2 + (r_{S3} + r_{S4})} \cdot d_3 \] (29)
Efficiency is given as:
\[ \eta = \frac{R(1-d_2)^2}{R(1-d_2)^2 + r_{L1}(1-d_2)^2 + r_{L2}d_2^2 + r_{S4}d_1 + r_{S2}d_2 + (r_{S3} + r_{S4})} \cdot d_3 \] (30)

For the conventional bidirectional SEPI/CZETA converter, actual conversion ratio and efficiency can be simply obtained by removing auxiliary current paths, thus now $d_3 = 0$ and $d_2 = 1-d_1$. For a forward SEPIC operation of the conventional SEPI/CZETA converter, actual voltage conversion ratio is obtained as:
\[ \frac{V_o}{V_{in}} = \frac{d_1}{1-d_1} \]
\[ \frac{R(1-d_1)^2}{R(1-d_1)^2 + r_{L2}d_1^2 + r_{L2}(1-d_1)^2 + r_{S1}d_1 + r_{S2}(1-d_1)} \] (31)
Efficiency is given by:
\[ \eta = \frac{R(1-d_1)^2}{R(1-d_1)^2 + r_{L2}d_1^2 + r_{L2}(1-d_1)^2 + r_{S1}d_1 + r_{S2}(1-d_1)} \] (32)
For a reverse ZETA operation of the conventional SEPIC/ZETA converter, actual voltage conversion ratio is obtained as:

\[
\frac{V_{in}}{V_o} = \frac{d_2}{1 - d_2}
\]

\[
\frac{R(1-d_2)^2}{R(1-d_2)^2 + r_{L1}(1-d_2)^2 + r_{L2}d_2^2 + r_{S1}(1-d_2) + r_{S2}d_2}
\] (33)

Efficiency is derived by:

\[
\eta = \frac{R(1-d_2)^2}{R(1-d_2)^2 + r_{L1}(1-d_2)^2 + r_{L2}d_2^2 + r_{S1}(1-d_2) + r_{S2}d_2}
\] (34)

In order to compare the actual voltage gains between the proposed converter and conventional bidirectional SEPIC/ZETA converter, following values of resistances are assumed and substituted into (27), (29), (31), and (33).

\[r_{L1}=r_{L2}=10\,\text{m}\Omega, \ r_{S1}=r_{S2}=r_{S3}=r_{S4}=5\,\text{m}\Omega, \ R=0.9\,\Omega.\]

Calculated actual voltage gains for the proposed converter and conventional SEPIC/ZETA converter in step-up and step-down modes are shown in Figs. 7 (a) and 7 (b), respectively. In the proposed converter, duty ratio of synchronous rectifier \(d_2\) for SEPIC and \(d_1\) for ZETA operations) is selected as small as 0.1 for the step-up mode. For the step-down mode, duty ratio of main switch \(d_1\) for SEPIC operation and \(d_2\) for ZETA operation) is chosen sufficiently small by 0.1. Those values are not dependent to the other duty ratios, which is not the case for the conventional SEPIC/ZETA converter. Owing to this design freedom, voltage gains of the proposed converter in both the step-up and step-down modes can be higher than those of conventional SEPIC/ZETA converter at the same duty ratio. Moreover, duty ratios \(d_1\) and \(d_2\) can be widely ranged in the proposed converter than conventional one.

Efficiencies for the proposed and conventional bidirectional SEPIC/ZETA converters are calculated assuming following parameters:

**Step-up:** \(r_{L1}=r_{L2}=10\,\text{m}\Omega, \ r_{S1}=r_{S2}=r_{S3}=r_{S4}=5\,\text{m}\Omega, \) voltage conversion from 14V to 17.3V

**Step-down:** \(r_{L1}=r_{L2}=10\,\text{m}\Omega, \ r_{S1}=r_{S2}=r_{S3}=r_{S4}=5\,\text{m}\Omega, \) voltage conversion from 21V to 17.3V

Substituting these parameters into (28), (30), (32), and (34), the calculated efficiencies are plotted in Fig. 8. Results show that the proposed converter has higher efficiency than conventional SEPIC/ZETA converter, especially in a higher power range, due to its possibility for optimized selection of duty ratios with respect to the conversion ratio.

V. **SOFT SWITCHING**

So far, we have treated the proposed converter as hard switched one for simple analysis. However, it indeed has soft switching features owing to the small inductor \(L_a\) on auxiliary current path. The soft current commutation aspect of the proposed converter in SEPIC operation mode is shown in Fig. 9. As mentioned in the analysis of Section II, \(S_1\) is turned off Fig. 7. Calculated voltage gains of the proposed converter and conventional bidirectional SEPIC/ZETA converter in (a) step-up and (b) step-down modes.

Fig. 8. Calculated efficiencies of the proposed converter and conventional bidirectional SEPIC/ZETA converter in (a) step-up and (b) step-down modes.
Fig. 9. Soft current commutation of the proposed converter in SEPIC operation.

after $t_0$ at the beginning of Mode 1. During this overlapped on-time between $S_1$ and $S_2$, the sum of $i_{L1}$ and $i_{L2}$ equals to the sum of $i_L$ and $i_{L1}$. The voltage of $L_a$ becomes $-V_o$ and $i_{L1}+i_{L2}$ can be assumed constant during this short time interval, thus

$$\frac{di_{S1}}{dt} = \frac{di_{La}}{dt} = \frac{V_o}{L_a}$$

(35)

Therefore $S_3$ and $S_4$ are turned off with current slope of $-V_o/L_a$, and $S_1$ is turned on with current slope of $V_o/L_a$. This soft current commutation takes time of $La(ILa(t_0)/V_o)$, thus $S_4$ should be turned off after this time interval for soft switching. This commutation time should be shorter than duration time of main switch for obtaining ZCS, thus

$$\frac{La(La(t_0))}{V_o} < dl$$

(36)

Similar phenomenon occurs at the beginning of Mode 3. After turning on of $S_3$ and $S_4$, sum of inductor currents $i_{L1}+i_{L2}$ is distributed to the $S_2$ and auxiliary current path through $S_3$ and $S_4$. During this commutation time, $i_{L1}+i_{L2}$ can be assumed constant and the voltage of $L_a$ becomes $V_{in}$, therefore

$$\frac{di_{S2}}{dt} = \frac{di_{La}}{dt} = \frac{V_{in}}{L_a}$$

(37)

$S_2$ is turned off with current slope of $-V_{in}/L_a$, thus diode reverse recovery problem is alleviated. $S_3$ and $S_4$ are turned on with current slope of $V_{in}/L_a$. This commutation process takes time of $La(La(t_2)/V_{in})$. $S_2$ should be turned off before $t_2$ for soft switching. For realizing ZCS, this commutation time should be shorter than duration time of auxiliary switches, thus

$$\frac{La(La(t_2))}{V_{in}} < dl$$

(38)

In summary, small inductor $L_a$ on auxiliary current path induces soft current commutation between switches, thus realizing ZCS of all switches. Similar development as above can be made for ZETA operation mode in the proposed converter. Besides this ZCS effect, ZVS turn-on and turn-off are also achieved at synchronous rectifiers, which are $S_2$ in SEPIC and $S_1$ in ZETA modes, respectively.

VI. SIMULATIONS AND EXPERIMENTS

To verify the operation of the proposed converter, a forward SEPIC operation of step-down case (from 21V to 17.3V) and a reverse ZETA operation of step-up case (from 14V to 17.3V) are simulated. Electric specifications are as follows: Output power $P_o=320W$ and switching frequency $f_s=100kHz$. In order to get the ripples of $i_{L1}$ and $i_{L2}$ to be 10% and 50%, respectively, inductors are selected by $L_1=L_2=30\mu H$. For the ripple voltages of $C_{in}$ ($\Delta v_{in}$), $C_o$ ($\Delta v_o$), and $C_s$ ($\Delta v_{Cs}$) to be 1%, 1%, and 2%, respectively, capacitors are chosen by $C_{in}=33\mu F$, $C_o=235\mu F$, and $C_s=440\mu F$. Considering actual switching duty ratios, those inductors and capacitors are determined by formulas in Table I. For the soft current commutation time of 200ns, $L_a$ is chosen to be 220nH. $S_1-S_4$ is IPP110N20N3 (200V, 88A, 10.7mΩ). In the simulation, a damping resistor of 50Ω is added in parallel with $L_a$ to attenuate parasitic oscillations occurring from $L_a$ and output capacitances of the switches. Simulation results are shown in Fig. 10. As expected, soft current commutation between switches has been noticed. ZCS turn-on and/or turn-off of switches can be also observed. With proper gating control ZVS turn-on and turn-off, and synchronous

Fig. 10. Simulation results of the proposed converter in (a) SEPIC step-down and (b) ZETA step-up operations.
rectifications are achieved in $S_2$ and $S_1$ for SEPIC and ZETA operations, respectively. Most importantly, inductor current ripples are highly reduced owing to a considerably reduced conduction times for main switch and synchronous rectifier, thereby reducing the dc resistive losses of inductors and capacitors, and conduction and switching losses of switches. A prototype circuit of the proposed converter (Fig. 11) has been built to verify the performance of the proposed converter. Electric specifications and circuit component values are the same with simulation. For the fair comparison between proposed converter and conventional bidirectional SEPIC/ZETA converter, some experimental waveforms such as inductor currents ($i_{L1}$, $i_{L2}$), switch currents ($i_{S1}$, $i_{S2}$, $i_{La}$), and switch voltages ($v_{S1}$, $v_{S2}$, $v_{S3}$, $v_{S4}$) are measured under the same electric specifications and circuit parameters. Those waveforms are shown in Figs. 12 and 13 for SEPIC step-down operation (from 21V to 17.3V) and shown in Figs. 14 and 15 for ZETA step-up operation (from 14V to 17.3V). Negative current polarity in ZETA operation means the reverse power flow. In SEPIC operation, inductor ripple current of proposed converter (2.19A) is reduced by 47% compared to that of conventional converter (4.14A). In ZETA operation, inductor ripple current is reduced by 32% from conventional SEPIC/ZETA (3.33A) to proposed converter (2.25A). For the proposed converter, soft current commutations between switches are confirmed and all switches achieved good ZCS property. On the other hand, the conventional SEPIC/ZETA converter showed hard switching behavior. Based on the measured switching voltages and currents, switching and conduction losses of switches have been calculated referring to [26]. Written here again, switching loss $P_{sw}$ is given as:

$$P_{sw} = (W_{on} + W_{off}) \cdot f_s$$

(39)

where $W_{on}$ and $W_{off}$ are energy lost during switching turn-on and turn-off transients, respectively. They are given by:

$$W_{on} = \frac{1}{2} V_p I_p t_{on}, \quad W_{off} = \frac{1}{2} V_p I_p t_{off}$$

(40)

where $V_p$ and $I_p$ are switching peak voltage and current during switching transients, respectively. $t_{on}$ and $t_{off}$ mean for time length of switching turn-on and turn-off transients, respectively. Conduction loss $P_{cond}$ is given by:

$$P_{cond} = I_{s,rms}^2 \cdot r_s$$

(41)

where $I_{s,rms}$ is rms current of switch in Table I and $r_s$ is on state drain-source resistance. Assuming $t_{on}$ and $t_{off}$ are both 50ns, switch losses of proposed and conventional converters...
obtained in Table II. As a result, overall conduction and switching losses of the proposed converter are lower than those of the conventional SEPIC/ZETA converter by 41%.

In voltage measurements of both proposed and conventional SEPIC/ZETA converters, large voltage spikes are observed at switching turn-off transient. They are caused by unclamped parasitic inductances of hardwired connectors in series with switches in prototype circuit which was built in breadboard. To eliminate these voltage spikes, power stack needs to be redesigned for reducing series inductance or some snubber circuit such as RC voltage snubber in [28] is required to suppress them. Focusing on the performance comparison between proposed and conventional converters, however, they are not considered in these experiments. Nonetheless when properly designed RC voltage snubber is applied to the circuit, voltage spike during turn-off transient would be effectively reduced with efficiency drop under 1%. For measurement of switch currents $i_{S1}$ and $i_{S2}$, $i_{S1} + i_{S2}$ is used instead of individual $i_{S1}$ and $i_{S2}$. For placing current probe, an artificial wire should be inserted in series with switch. Its small inductance induces unwanted parasitic oscillation with parasitic capacitances of circuit components and also results in high voltage spike during switching turn-off transient. To avoid those effects, therefore, switch currents $i_{S1}$ and $i_{S2}$ are extracted using mathematical functions of oscilloscope such as sum and subtraction, i.e. $i_{S1} + i_{S2} = i_{L1} + i_{L2} - i_{La}$. In $i_{S1} + i_{S2}$, $i_{S1}$ and $i_{S2}$ are easily distinguished from the current slope change.

Measured efficiencies for the two converters are shown in Fig. 16 as black lines. In average, the efficiency of the proposed converter is 5% higher than that of conventional one. Efficiency difference between two converters is proportional to output power because of the increased conduction and switching losses of the circuit components in high current range. Due to the laboratorial limitation, thermal design for heat radiation of switches and inductors does not considered in

<table>
<thead>
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<th>Power loss</th>
<th>SEPIC step-down</th>
<th>ZETA step-up</th>
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<tbody>
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<td></td>
<td>Conventional</td>
<td>Proposed</td>
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<td>Switching loss</td>
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<td>Conduction loss</td>
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<td>8.02</td>
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<tr>
<td>Total switch loss</td>
<td>19.65</td>
<td>10.29</td>
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</table>
this prototype circuit. Therefore, efficiency curve shows rapid drop in values in high power range. Assuming that a proper thermal design is implemented thus there is no efficiency degradation from thermal issue, ideal efficiency curve can be expected using loss analysis including switching and conduction losses of switches and dc resistive losses of inductors. Switch losses can be calculated using (39), (40), and (41). Dc resistive losses of inductors, $P_L$, are determined by:

$$P_L = I_{L, \text{rms}}^2 \cdot r_L \quad (42)$$

where $I_{L, \text{rms}}$ is rms current of inductor in Table I and $r_L$ is dc resistance of inductors of 5mΩ. Those results are shown in Fig. 16 as gray lines. At $P_o=650$W, ideal calculated efficiency of proposed converter is 3.5% higher than measured one.

VII. CONCLUSIONS

This paper researches a new nonisolated bidirectional soft switching SEPIC/ZETA converter which can reduce ripple currents in inductors. The proposed converter has following advantages. 1) Inductor currents have much reduced ripple due to the reduced duration times of main switch and synchronous rectifier. 2) ZCS turn-on and/or turn-off are achieved in all switches with soft current commutation among them. 3) Synchronous rectification and ZVS turn-on and turn-off are achieved in synchronous rectifier. 4) Voltage gains in both step-up and step-down modes can be higher than those of conventional bidirectional SEPIC/ZETA converter owing to the optimized duty ratios of switches. As a result, conduction and switching losses in circuit components were considerably reduced. Lower current rated switches can be also utilized. Filter size can be also minimized. In the experimental results of prototype circuit, operation waveforms and soft switching properties are well agreed with theoretical analysis and simulation results. Measured inductor ripple currents are reduced by 40% and overall efficiency of the proposed converter is 5% higher than the conventional bidirectional SEPIC/ZETA converter, demonstrating the effectiveness of the proposed converter.

REFERENCES


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