PWM Control Techniques for Single-Phase Multilevel Inverter Based Controlled DC Cells

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Abstract

This paper presents a single-phase five-level inverter controlled by two novel Pulse Width Modulation (PWM) switching techniques. The proposed PWM techniques have been designed based on minimum switching power loss and minimum Total Harmonic Distortion (THD). In a single-phase five-level inverter employing six switches, the first PWM proposed technique requires four switches operate at switching frequency and the other two switches at line frequency, whereas the second PWM proposed technique requires only two switches operate at switching frequency and the others operate at line frequency. Compared with conventional PWM techniques for single-phase five-level inverter, both of the proposed PWM techniques have the merits of high efficiency and low harmonic contents in the output voltage. The validity of the proposed PWM switching techniques for controlling the single-phase five-level inverter to regulate load voltage have been verified experimentally using laboratory prototype based 100V, 500W controlled by dspace-1103.

Key words: Multilevel inverter, single-phase inverter, PWM, voltage control.

I. INTRODUCTION

Recently, the applications of power electronics inverters are becoming increasingly important. PWM inverters have the ability to control their output voltage and frequency, simultaneously. Therefore PWM inverters are considered power candidate in the industrial applications such as renewable energy sources, electrical machine drives, uninterrupted power supplies, and power conversion applications. Since high efficiency and low harmonic contents are becoming increasingly important, they introduce new requirements for the PWM inverters switching techniques and circuit topologies. The most important issues raised in these studies are the output voltage levels and the limitation of switching devices [1], [2].

Multilevel inverters are increasingly being considered for power electronics applications due to their ability to operate higher output voltage while producing lower levels of harmonic components in the switched output voltage since it has a greater availability of voltage levels [3]–[9]. Also, the output voltages can be filtered using smaller reactive components. Moreover, the switching frequencies of the devices can be reduced and more sinusoidal shaped output voltage waves can be obtained [10], [11]. Multilevel inverters is now preferred in high power medium voltage applications due to the reduced voltage stresses on the devices. Neutral Point Clamped (NPC) [12], [13], Flying capacitors [14]–[16], and cascaded H-bridge inverters [17]–[19] are considered the most famous topologies of the multilevel inverters. However, the most particular disadvantages of these multilevel inverter topologies are the large number of the required power semiconductor switches resulting in high switching power loss. Although low voltage rate switches can be utilized in a multilevel inverter, each switch requires a gate drive circuit. This may cause the overall system to be more expensive and complex. So, in practical implementation, reducing the number of switches and hence gate driver circuits have become an essential research topic [20].

Recently, many topologies of the single-phase multilevel inverter and its PWM switching techniques have been published. In [20], combinations of series and parallel switches have been used to implement the multilevel inverter. However, this topology uses large number of power switches. In [21], the multilevel inverter is implemented by using two switches and two power diodes with the H-bridge single phase inverter. Those two systems can generate only five levels in the output voltage. In [22], the conventional single-phase inverter is converted to a single-phase five level inverter by adding one switch and four power diodes to the conventional H-bridge single phase inverter. In [23], a modular inverter that can produce any required voltage levels has been presented. In [24], single-phase five-level inverter has been proposed using only six power switches in addition two coupled inductors and only one dc supply. However, the size of the coupled inductors is large. In [25], the idea of single-phase five-level inverter has been presented using only six power switches in addition to two floating dc power supplies. However, its control scheme has been designed based on lookup table. In [26], the idea of a new topology of a single-phase five-level inverter has been
presented based on minimum number of power switches. It adopts full-bridge configuration by employing single pulse control technique based switching angles calculation method. The harmonic components of the output voltage are determined by the load inductance in addition to the filter. Therefore, their harmonic reduction is limited to a certain degree. Furthermore, the technique of switching angles calculation method requires on-line calculations of the switching angles and a lookup table. The same technique has been modified in [27] by using bidirectional switches, which increases the number of power switches used in the cascaded controlled dc cells. In [28], the same technique has been used to obtain a single-phase multilevel inverter using conventional power switches. However, each dc supply has been controlled by two switches. To overcome these limitations, in [29], the authors have proposed a new PWM switching technique for controlling the single-phase five-level inverter based on high efficiency and low harmonics.

Motivated by the aforementioned issues, this paper presents two novel control PWM switching techniques for controlling a stand-alone single-phase five-level inverter. The structure of the inverter uses two power switches controlling the dc input voltage of a conventional H-bridge inverter. In both control schemes, some switches operate at high switching frequency and the others operate at fundamental line frequency in order to reduce the switching power loss. Proportional-Integral (PI) controller is used to achieve load voltage to be same as the reference one. Theoretical analysis, numerical simulation and laboratory prototype with several experimental results are presented in order to investigate the capability of the proposed PWM switching schemes in controlling the load voltage in addition to confirm the characteristics of the proposed inverter.

II. CONFIGURATION AND OPERATIONAL PRINCIPLE OF THE PROPOSED INVERTER

The proposed structure of the single-phase multilevel inverter is shown in Fig. 1. It consists of n-cells connected in series, one cell is a dc supply whereas the other cells have dc supply controlled by two switches \( (S_{k1},S_{k2}) \), where \( k = 1, 2, \ldots, n \). The switch \( S_{k2} \) is connected in series with the dc voltage source and the other switch \( S_{k1} \) is connected in parallel with both the dc voltage source and the series switch \( S_{k2} \). According to the proposed configuration shown in Fig. 1, each cell controlled by two switches has two output voltage states; zero voltage and the dc voltage source associated with the considered cell. Since cell-n has only dc voltage source, it has only one state voltage which is the value of its dc supply. Therefore, the dc bus voltage has \( (n) \) states based on the values of \( (V_1, V_2, \ldots, V_n) \), as shown in Fig. 2. It is cleared that the dc bus shown in Fig. 1 has no zero state voltage. Therefore, cell-n is the basic cell that must be included at any multilevel inverter based on the proposed topology.

![Fig. 1. Configuration of single-phase multilevel inverter.](image)

Conventional H-bridge inverter is connected at the dc bus terminals to convert the dc voltage to switched bipolar voltage limited by the value of dc voltage at the dc bus. The H-bridge inverter consists of four switches \( (Q_1, Q_2, Q_3, \text{and } Q_4) \), as shown in Fig. 1. The main function of the H-bridge inverter is to obtain the zero state voltage on the ac load by considering the switches \( Q_1 \) and \( Q_3 \) or \( Q_2 \) and \( Q_4 \) to be on, simultaneously, in addition to obtaining the positive half-cycle by considering the switches \( Q_1 \) and \( Q_2 \) to be on and the negative half-cycle by considering the switches \( Q_3 \) and \( Q_4 \) to be on. Obviously, this structure can reduce the number of switches compared to the conventional topologies used in single-phase multilevel inverter without affecting the inverter performances, since the zero state voltage can be generated using either the upper or lower switches of the H-bridge inverter.

III. PROPOSED SINGLE-PHASE FIVE-LEVEL INVERTER

In order to generate five levels of the proposed inverter shown in Fig. 1, the number of the required cascaded cell is two; \( (n = 2) \). One cell has a dc supply controlled by two switches and the other cell has only a dc supply.
IV. SWITCHING ALGORITHMS FOR THE PROPOSED PWM SWITCHING TECHNIQUES

Switching frequency and ON-OFF terminal voltage of power semiconductor devices are the main factors affecting the inverter power loss and harmonic contents. Motivated by that, two PWM switching techniques are proposed to control the single-phase five-level inverter. Switching loss and harmonic distortion have been considered in both techniques by operating some switches at high frequency and the others at fundamental line frequency.

A. Technique-I

The first proposed PWM switching technique for the single-phase five-level inverter is basically depending on generating gate signals by comparing rectified reference waveform with two in-phase triangle carriers having same frequency, same peak-to-peak, but different offset voltages. Fig. 5 shows the switching patterns of the single-phase five-level inverter using PWM Technique-I. The intersection points between carrier A and carrier B with the reference waveform decide the inverter output voltage level. The first level of the inverter output voltage ±V_{dc} is generated at the intersection points of the reference voltage waveform and the lower carrier signal (carrier A), whereas the second level of the output voltage ±2V_{dc} is generated at the intersection points of the reference voltage waveform and the upper carrier signal (carrier B). The positive half-cycle of the reference voltage waveform is responsible for generating the positive dc voltage levels (V_{dc} and 2V_{dc}) in the output voltage, whereas the rectified half-cycle is responsible for generating the negative dc voltage levels (−V_{dc} and −2V_{dc}).

According to the reference voltage, the intersection with the carrier may happen with the lower carrier only resulting in modulation index between zero and 0.5, or with both carrier signals resulting in modulation index between 0.5 and 1. Therefore, if the modulation index is less than or equals 0.5, the output voltage of the inverter will have only three levels (V_{dc}, 0, and −V_{dc}). On the other hand, if the modulation index is more than 0.5, the output voltage of the inverter will have five levels (2V_{dc}, V_{dc}, 0, −V_{dc}, and −2V_{dc}). According to the amplitude of the reference voltage, its period can be divided into five intervals based on four modes (Mode A, Mode B, Mode C, and Mode D). Based on the related displacement phase angles (θ_1, θ_2, θ_3, and θ_4), shown in Fig. 5, the operational modes can be defined as follows:

\[
\begin{align*}
\text{Mode A} & \quad 0 < \omega t < \theta_1, \quad \theta_1 < \omega t \leq \pi \\
\text{Mode B} & \quad \theta_1 < \omega t \leq \theta_2 \\
\text{Mode C} & \quad \pi < \omega t < \theta_3, \quad \theta_3 < \omega t \leq 2\pi \\
\text{Mode D} & \quad \theta_3 < \omega t \leq \theta_4
\end{align*}
\]  

The modulation index (MI) of the proposed single-phase five-level inverter is defined as follows:

Fig. 3 shows the configuration of the proposed single-phase five-level inverter. Two switches are added to the conventional single-phase H-bridge inverter in order to perform a single-phase five-level inverter. In order to achieve a balanced output voltage levels, the dc voltage sources in both cells are typical; V_1 = V_2 = V_{dc}. The load level output voltage V_{ab} will have two states: V_{dc} and 2V_{dc}. The load output voltage V_{ab} will have five states: (2V_{dc}, V_{dc}, 0, −V_{dc}, and −2V_{dc}).

The load voltage zero state can be generated either by switching simultaneously the upper switches or the lower switches of the H-bridge inverter. The other four states can be generated from the DC Bus voltage V_{bus}.

Since the load current is bi-directional regardless of the load voltage, operation of the proposed single-phase five-level inverter has 10 switching states, as illustrated in Fig. 4 and Table I. The switching patterns of the proposed inverter are shown in Fig. 4, whereas the load current directions at each load voltage level state according to switch ON-OFF conditions are shown in Table I. The conventional freewheeling states (zero voltage states) are shown in Fig. 4 (e) and (f). The other output voltage levels even + or − can be achieved by switching the conventional H-bridge inverter with the control of cell-1 switches (S_{11} and S_{12}). PWM switching technique is required to control the single-phase five-level inverter to achieve the reference load voltage based on the 10 switching patterns shown in Fig. 4 and Table I.

### Table I

<table>
<thead>
<tr>
<th>States</th>
<th>V_{ab}</th>
<th>i_o</th>
<th>ON switches</th>
</tr>
</thead>
<tbody>
<tr>
<td>a</td>
<td>2V_{dc}</td>
<td>+</td>
<td>Q1, Q2 and S_{12}</td>
</tr>
<tr>
<td>b</td>
<td>2V_{dc}</td>
<td>−</td>
<td>D1, D2 and S_{12}</td>
</tr>
<tr>
<td>c</td>
<td>V_{dc}</td>
<td>+</td>
<td>Q1, Q2 and S_{11}</td>
</tr>
<tr>
<td>d</td>
<td>V_{dc}</td>
<td>−</td>
<td>D1, D2 and S_{11}</td>
</tr>
<tr>
<td>e</td>
<td>−V_{dc}</td>
<td>+</td>
<td>Q3 and D3 or Q3 and D2</td>
</tr>
<tr>
<td>f</td>
<td>−V_{dc}</td>
<td>−</td>
<td>Q3, Q4 and S_{11}</td>
</tr>
<tr>
<td>g</td>
<td>−2V_{dc}</td>
<td>+</td>
<td>D3, D4 and S_{12}</td>
</tr>
</tbody>
</table>

Fig. 3. Model of single-phase five-level inverter.
where $A_M$ is the peak value of the reference modulating waveform, and $A_C$ is the peak-to-peak value of the carrier. Also, the frequency ratio ($m_f$) is defined as follows:

$$m_f = \frac{f_c}{f_m}$$

where $f_c$ is the frequency of the carrier signals, and $f_m$ is the frequency of the modulating signal.

Fig. 5 shows that the displacement phase angles ($\theta_1$, $\theta_2$, $\theta_3$ and $\theta_4$) are affected by the modulation index ($M_I$). If the modulation index is less than or equal 0.5, the displacement phase angles will be defined as follows:

$$\theta_1 = \theta_2 = \frac{\pi}{2}, \quad \theta_3 = \theta_4 = \frac{3\pi}{2}$$

If the modulation index is greater than 0.5, the displacement phase angles will be defined as follows:

$$\begin{align*}
\theta_1 &= \sin^{-1}\left(\frac{A_C}{A_M}\right) \\
\theta_2 &= \pi - \theta_1 \\
\theta_3 &= \pi + \theta_1 \\
\theta_4 &= 2\pi - \theta_1
\end{align*}$$

According to the intersections between the modulation waveform and the carrier signals, the period of the reference voltage ($2\pi$) is divided into six time intervals defined as ($P_1$, $P_2$, $P_3$, $P_4$, $P_5$ and $P_6$), as shown in Fig. 5. The signals $C_A$ and $C_B$, shown in Fig. 5 result from comparing the modulation waveform with the lower and upper triangle carriers, respectively. The gate signals of the proposed inverter switches can be calculated based on the resultant signals $C_A$ and $C_B$ in addition to the six time intervals ($P_1$, $P_2$, $P_3$, $P_4$, $P_5$, and $P_6$). The resultant gate signals of the inverter six switches can be formulated as follows:

$$
\begin{align*}
Q_1 &= P_1 + P_2 + P_3 \\
Q_2 &= (P_1 + P_2 + P_3) \cdot C_A + (P_4 + P_5) \cdot C_A \\
Q_3 &= (P_1 + P_3) \cdot C_A + (P_4 + P_5 + P_6) \cdot C_A \\
Q_4 &= P_4 + P_5 + P_6 \\
S_{11} &= ((P_1 + P_3) + (P_4 + P_6)) \cdot C_A + (P_2 + P_3) \cdot C_B \\
S_{12} &= (P_2 + P_5) \cdot C_B
\end{align*}
$$

It is cleared from (6) and Fig. 5 that the inverter power switches ($Q_1$ and $Q_4$) are complementary switches operating at the fundamental line frequency (i.e. 50 Hz). Also, the power switches ($S_{11}$ and $S_{12}$) cannot switching ON simultaneously. However, their switching signals are decided based on (6) and operating at switching frequency. Moreover, the power switches ($Q_2$ and $Q_3$) are complementary switches operating at switching frequency.

**B. Technique-II**

The second proposed technique presents more simplicity for controlling the single-phase five-level inverter. Technique-II uses only two switches operating at switching frequency and the other four switches operate at the fundamental line frequency. Fig. 6 shows the switching patterns of the single-phase five-level inverter using PWM technique-II. This technique is basically depending on generating gate signals by comparing rectified reference waveform with two in-phase triangle carriers having same frequency, no offset voltage, but the peak-to-peak voltage of carrier B is double that of carrier A. The intersections between reference voltage waveform and carrier A generate the first level ($\pm V_{dc}$) at the output of the inverter, whereas the intersections between reference voltage waveform and carrier B generate the second level ($\pm 2V_{dc}$). The zero voltage level at the inverter output can be generated using the upper or lower switches of the H-bridge, same as that in Technique-I. Also, the positive dc output voltage levels ($V_{dc}$ and $2V_{dc}$) are generated by the positive half-cycle of the reference waveform, whereas the voltages ($-V_{dc}$ and $-2V_{dc}$) are generated by the rectified half-cycle of the reference waveform. Since the two carriers have no offset voltage, the reference waveform has intersection points with both carriers simultaneously. However, the modulation index is defined to be 0.5 at the peak voltage of carrier A. Therefore, if the modulation index is less than or equal 0.5, the output voltage of the inverter will have only three levels, same as that of Technique-I, ($V_{dc}$, 0, and $-V_{dc}$). On the other hand, if the modulation index is more than 0.5, the output voltage of the inverter will have five levels ($2V_{dc}$, $V_{dc}$, 0, $-V_{dc}$, and $2V_{dc}$), as shown in Fig. 6.

The results of comparing the reference waveform with carrier A and carrier B are shown in Fig. 6 given in signals $C_A$ and $C_B$, respectively. Based on the peak value of the reference voltage waveform, the period ($2\pi$) is divided into six time intervals defined as ($P_1$, $P_2$, $P_3$, $P_4$, $P_5$, and $P_6$), as shown in Fig. 6 and same as that in Technique-I.

Based on the resultant signals $C_A$ and $C_B$ in addition to the six time intervals ($P_1$, $P_2$, $P_3$, $P_4$, $P_5$, and $P_6$), the resultant gate signals of the inverter six switches can be formulated as follows:

$$
\begin{align*}
Q_1 &= P_1 + P_2 + P_3 \\
Q_2 &= ((P_1 + P_3) \cdot C_A) + (P_4 + P_6) \cdot C_A \\
Q_3 &= (P_4 + P_6 + P_5) \cdot C_A \\
Q_4 &= P_4 + P_5 + P_6 \\
S_{11} &= (P_1 + P_3) + (P_4 + P_6) \cdot C_A + (P_2 + P_3) \cdot C_B \\
S_{12} &= (P_2 + P_5) \cdot C_B
\end{align*}
$$
Fig. 4. Operational switching states of the proposed single-phase five-level inverter and the direction of load current.

(a) $v_o = 2V_{dc}$, $i_o = (+)$

(b) $v_o = 2V_{dc}$, $i_o = (-)$

(c) $v_o = V_{dc}$, $i_o = (+)$

(d) $v_o = V_{dc}$, $i_o = (-)$

(e) $v_o = 0$, $i_o = (+)$

(f) $v_o = 0$, $i_o = (-)$

(g) $v_o = -V_{dc}$, $i_o = (+)$

(h) $v_o = -V_{dc}$, $i_o = (-)$

(i) $v_o = -2V_{dc}$, $i_o = (+)$

(j) $v_o = -2V_{dc}$, $i_o = (-)$
It is cleared from the switching pattern of Technique-II, shown in Fig. 6, that the cell switches controller ($S_{11}$ and $S_{12}$) are complement to avoid short circuit on the dc voltage supply and operate at the double line frequency. Also, two switches of the H-bridge inverter ($Q_1$ and $Q_2$) operate complementary at the line frequency. Therefore, Technique-II provides PWM switching for six power switches with only two of them operate at high frequency.

Therefore, both of the proposed PWM techniques provide an output voltage that has five levels. The voltage difference during switching of any power switch in Technique-I is $V_{dc}$ at any time. On the other hand, the inverter output voltage in Technique-I changes from zero to $2V_{dc}$ at the time interval period $P_2$, or from zero to $-2V_{dc}$ at the period $P_5$, providing switching at higher voltage than that given by Technique-I. This in turn results in higher switching loss and harmonics compared with that in Technique-I.

**V. HARMONIC ANALYSIS OF THE PROPOSED PWM PATTERNS**

The harmonic components and Total Harmonic Distortion (THD) of output voltages in the proposed two techniques are presented here. Fig. 5 indicates that the output voltage waveforms of both techniques are odd quarter-wave symmetry ($a_n = 0$).
Therefore, the THD of the output voltage waveform can be formulated as follows:

\[
THD = \frac{4}{\pi B_1} \left( \sum_{n=3}^{\infty} \left( \frac{1}{n} \right)^{0.5} \left[ \sum_{k=1}^{M_1} (-1)^{k+1} \cos(n\alpha_k) + 2\sum_{k=1}^{M_2} (-1)^{k+1} \cos(n\beta_k) \right] \right)^{0.5}
\]

(10)

where \( n \) is odd orders \((n=3, 5, \ldots)\).

B. THD of Technique-II

The Fourier series of the inverter output voltage waveform based on Technique-II can be expressed as follows:

\[
f(w) = \frac{4V_{dc}}{\pi B_1} \left[ \sum_{k=1}^{M_1} \sum_{n=1}^{\infty} (-1)^{k+1} \cos(n\alpha_k) \sin(n\omega t) + 2\sum_{k=1}^{M_2} \sum_{n=1}^{\infty} (-1)^{k+1} \cos(n\beta_k) \sin(n\omega t) \right]
\]

(11)

The fundamental frequency amplitude at \( n = 1 \) is formulated as follows:

\[
B_1 = \frac{4V_{dc}}{\pi} \cos(\alpha_k) + \frac{8V_{dc}}{\pi} \cos(\beta_k)
\]

(12)

where:

\[
\begin{align*}
&n = 1, 3, 5, \ldots \\
&90^o = \alpha M_1 > \ldots > \alpha 3 > \alpha 2 > \alpha 1 \\
&90^o = \beta M_1 > \ldots > \beta 3 > \beta 2 > \beta 1
\end{align*}
\]

Therefore, the THD of the output voltage waveform can be formulated as follows:

\[
THD = \frac{4}{\pi B_1} \left( \sum_{n=3}^{\infty} \left( \frac{1}{n} \right)^{0.5} \left[ \sum_{k=1}^{M_1} (-1)^{k+1} \cos(n\alpha_k) + 2\sum_{k=1}^{M_2} (-1)^{k+1} \cos(n\beta_k) \right] \right)^{0.5}
\]

(13)

where \( n \) is odd orders \((n=3, 5, \ldots)\).

By using (10) and (13), the THD of the proposed PWM techniques is calculated and it will be compared with simulation and experimental in the following section.

VI. CONTROL SCHEME

The single-phase five-level inverter employing LC filter is applied to control the voltage at a resistive load. Fig. 7 shows the control scheme of the single-phase five level inverter for regulating the resistive load voltage \((v_L)\). A simple LC filter is used to obtain a sinusoidal voltage waveform at the load. Since the inverter output voltage has five levels, the parameters of the LC filter are small compared with that used in conventional three-level inverters.

The implemented control scheme shown in Fig. 7 is used to investigate the ability of the proposed PWM techniques (Technique-I and Technique-II) to drive the single-phase five-level inverter. Conventional Proportional-Integral (PI) controller is used to regulate the load voltage to be same as the sinusoidal reference one \((v_L^*)\), as shown in Fig. 7. Therefore, the actual load voltage \((v_L)\) is compared with the reference voltage \((v_L^*)\) and the error is minimized using the PI controller. The modulation index \((M1)\) is the output of the PI controller. The \(M1\) is compared with the two carriers in each technique to generate pulses \((C_{a0}, C_{b0}, P_1, P_2, P_3, P_4, P_5,\text{ and } P_6)\). Then, Equs. (6) and (7) are used to generate inverter switches pulses for technique-I and -II, respectively.

Therefore, the actual load voltage \((v_L)\) is compared with the reference voltage \((v_L^*)\) and the error is minimized using the \(M1\) controller. The modulation index \((M1)\) is the output of the \(M1\) controller. The \(M1\) is compared with the two carriers in each technique to generate pulses \((C_{a0}, C_{b0}, P_1, P_2, P_3, P_4, P_5,\text{ and } P_6)\). Then, Equs. (6) and (7) are used to generate inverter switches pulses for technique-I and -II, respectively.

VII. SIMULATION RESULTS

The single-phase five-level inverter and its two proposed PWM switching techniques have been carried out using Matlab/Simulink in order to verify the validity of the topology. The simulated system is controlled using conventional PI controller as shown in Fig. 7. Ideal power switches have been used to simulate the inverter circuit. The parameters of the simulated system are shown in Table II. Based on the modulation index, the inverter output voltage can be three or five levels. Both low and high modulation index is used to verify the validity of the proposed two PWM techniques in controlling the load voltage. The reference load voltage \((v_L^*)\) is set as 43 V (RMS) with a modulation index about 0.4 to investigate the three-level output voltage, whereas \((v_L^*)\) is set as 100 V (RMS) with a modulation index about 0.9 to investigate the five-level output voltage.

A. Simulation results using Technique-I

Fig. 8 shows the simulation results of the inverter output voltage \((v_L)\), actual and reference load voltage \((v_L, v_L^*)\), and the load current \((i_L)\) during three-level output voltage control.
It is cleared that the inverter output voltage has only three levels of \((0, \pm 80)\). Also, the reference and actual load voltage coincide well. Moreover, the load voltage and current are sinusoidal waveforms with low ripples. On the other hand, the simulation results of the five-level output voltage is shown in Fig. 9 during controlling the output voltage to be equal 141 V (RMS). It is cleared that the inverter output voltage has five levels of \((0, \pm 80, \pm 160)\), and the reference and actual load voltage looks identical. Moreover, the ripples in the sinusoidal waveforms of the load voltages and currents are reduced, since the inverter output voltage levels are increased.

Fig. 8. Simulation results of the single-phase five-level inverter at \(v_L^* = 42.4V\) (RMS) using PWM technique-I.

Fig. 9. Simulation results of the single-phase five-level inverter at \(v_L^* = 100 V\) (RMS) using PWM technique-I.

Fig. 10. Simulation results of the single-phase five-level inverter at \(v_L^* = 42.4V\) (RMS) using PWM technique-II.

Fig. 11. Simulation results of the single-phase five-level inverter at \(v_L^* = 100 V\) (RMS) using PWM technique-II.

Fig. 12. Experimental system configuration.
**B. Simulation results using Technique-II**

Fig. 10 and Fig. 11 show the simulation results of the system when the reference load voltage is set as 43 V (RMS) and 100 V (RMS), respectively, using PWM technique-II. In both figures, the reference and actual load voltages agree well and the sinusoidal waveforms of the load voltage and current have low ripples. Also, the inverter output voltage shown in Fig. 10 has only three levels of (0, ±80) since the modulation index in less than (0.5), whereas the inverter output voltage in Fig. 11 has only five levels of (0, ±80, and ±160) since the modulation index is higher than (0.5).

The three-level output voltage obtained using PWM technique-II is similar to that obtained using PWM technique-I, since the power switches are ideal. However, the ripples of the load voltage and currents in Fig. 11 are higher than that obtained from the other cases, since the five levels, obtained by PWM technique-II, are always step from zero, which in turn increases the load voltage harmonics and the voltage stress on power switches.

**VIII. EXPERIMENTAL RESULTS**

Laboratory prototype systems have been carried out in order to demonstrate the effectiveness of the single-phase five-level inverter for controlling the load voltage. The proposed two PWM techniques have been used to confirm their capabilities in driving the inverter. Experimental waveforms of the load current, load voltage, and inverter output voltage in both techniques have been captured. Harmonic components and THD in both techniques have been measured and compared with the theoretical values in order to demonstrate the accuracy of the experimental system and the proposed control schemes.

**A. Experimental system configuration**

Fig. 12 shows the laboratory prototype of the single-phase five-level inverter with its two dc supplies in the input, LC filter at the output, resistive load, and the digital controller. Fig. 13 shows the laboratory prototype system photograph. The dspace 1103 is selected as the controller for the single-phase five-level inverters. This inverter has been built with MOSFET IRFP31N50L as the power device. The switching frequency for inverters is 10 kHz. The parameters of the whole system are listed in Table II. The captured experimental waveforms of the inverter output voltage in addition to the load voltage and current has been measured using Tektronic MSO2000 Oscilloscope. Efficiency of the inverter and inverter harmonic components of its output have been measured using Yokogawa digital power analyzer WT1800. The main function of the single-phase five-level inverter employing LC filter is to control the load voltage \( v_L \) to be same as the reference sinusoidal one \( v_r \) using conventional PI control technique. Therefore, only one voltage sensor is needed to detect the actual load voltage that is compared with the reference one inside the controller to obtain all switches gate signals based on the generated modulation index and the two carriers.

Fig. 13. Experimental system prototype.

**TABLE II**

<table>
<thead>
<tr>
<th>Simulation and Experimental System Parameters</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Source voltage ( V_{inv} )</td>
<td>80 V</td>
</tr>
<tr>
<td>Load ( R_L )</td>
<td>23 Ω</td>
</tr>
<tr>
<td>Filter ( L_f )</td>
<td>1.0 mH</td>
</tr>
<tr>
<td>( C_f )</td>
<td>470 μF</td>
</tr>
<tr>
<td>Switching time ( T_s )</td>
<td>100 μS</td>
</tr>
<tr>
<td>Main PI gains ( K_P, K_I )</td>
<td>0.01 A/V, 0.005 A/V.sec</td>
</tr>
</tbody>
</table>

Both of the proposed PWM techniques, Technique-I and Technique-II, have been used to control the single-phase five-level inverter in order to demonstrate their effectiveness in controlling the load voltage in addition to investigate their power quality. In each technique, two different voltage levels have been confirmed in order to examine the inverter behavior at different modulation indices. Reference load voltage has been adjusted to be 43 V (RMS) and 100 V (RMS) with a modulation index of 0.4 and 0.9, respectively. At the modulation index of 0.4 (less than 0.5), the behavior of the inverter is similar to the conventional full-bridge three-level inverter, whereas at the modulation index of 0.8 (greater than 0.5), the inverter output voltage has five levels.

**B. Load voltage control using Technique-I**

The laboratory prototype shown in Fig. 12 has been carried out using the PWM technique-I in order to control the single-phase five-level inverter supplying an AC resistive load. Fig. 14 shows the experimental results of the system in case of load reference voltage equal to 43 V (RMS) with a modulation index about 0.4 and the inverter output voltage has three levels. Fig. 14 (a) shows the inverter output voltage \( v_{inv} \), reference and actual load voltage \( v_r, v_L \), and load current \( i_L \). It is cleared that the reference and actual load voltage looks identical.
Fig. 14. Experimental results of the single-phase five-level inverter at \( v^*_L = 42.4 \text{ V (RMS)} \) using PWM technique-I.

Fig. 14 (b) and (c) show the inverter output voltage and load voltage after the LC filter with their FFT showing their harmonic contents. It is cleared that the LC filter has removed the harmonics of the inverter output voltage and provides the load with sinusoidal voltage waveform. THD of the inverter output voltage and the load voltage are 75.1% and 5.9%, respectively. Fig. 14(d) shows the power analyzer results of the load voltage, current, and inverter voltage in addition to the system efficiency. The efficiency of the system is 77.9%.

Fig. 15 shows the experimental results of the system in case of load reference voltage equal to 100V (RMS) with a modulation index about 0.9 and the inverter output voltage has five levels.

It is cleared that the actual load voltage coincides with the reference one. The harmonic components of inverter output voltage shown in Fig. 15 (b) is less than that shown in Fig. 14 (b) due to the increase in the output voltage levels (target operation). THD of the inverter output voltage and the load voltage are 39.6% and 3%, respectively. Moreover, the efficiency of the system operating at the five-level mode is higher than that operating in the three-level mode due to the harmonic reduction. The measured efficiency of the system is 90.7%.

C. Load voltage control using Technique-II

The laboratory prototype has been carried out in order to investigate the effectiveness of the proposed PWM
Technique-II under the same conditions of Technique-I.

The reference voltage is adjusted using the same two voltage used in Technique-I (43 V and 100 V) in order to compare the power quality of the proposed two techniques.

Fig. 16 shows the experimental results of the single-phase five-level inverter at \( v_{L} = 42.4 \text{ V (RMS)} \) using PWM technique-II. The reference voltage is equal to 43 V (RMS) with a modulation index less than (0.5). The reference and actual load voltage, shown in Fig. 16 (a), coincides well. The harmonic contents of the inverter output voltage and load voltage using FFT are shown in Fig. 16 (b) and (c). THD of the inverter output voltage and the load voltage are 74.4% and 5.6%, respectively. The system efficiency has been measured using digital power analyzer as shown in Fig. 16 (d). The efficiency of the system is 78.5%.

Fig. 17 shows the experimental results of the system using PWM Technique-II in case of load reference voltage equal to 100 V (RMS) with a modulation index (0.5 < \( M_{l} \leq 1 \)). It is cleared that the actual load voltage coincides with the reference one. The inverter voltage has been changed from 0 level to \( \pm V_{dc} \) during the intersection between the modulation waveform and carrier A and from 0 level to \( \pm 2V_{dc} \) during the intersection with carrier B. Since the voltage levels have been increased to five, the harmonic components of inverter output voltage shown in Fig. 17(b) is less than that shown in Fig. 16(b). The load voltage harmonics is shown in Fig. 17(c). THD of the inverter output voltage and harmonic distortion FFT are shown in Fig. 17 (b) and (c).
voltage and the load voltage are 52% and 3.6%, respectively. Moreover, the efficiency of the system is higher than that of the three-level mode due to the harmonic reduction. The efficiency of the system is 88.3%.

Fig. 18 shows a comparison between the simulation and experimental results of the Total Harmonic Distortion (THD) of the inverter output voltage $V_{in}$ controlled by PWM Technique-I with the variation of modulation index.

Fig. 19 shows the same comparison of the THD using PWM Technique-II. It is cleared that both techniques have nearly same THD when the modulation index is less than 0.5 ($0 < M_I \leq 0.5$) since the inverter output voltage is almost same, having conventional three levels. However, when the modulation index is higher than 0.5 ($M_I > 0.5$), THD in the inverter output voltage controlled by PWM technique-I is less than that obtained by using PWM Technique-II. This is due to the change in inverter voltage controlled by Technique-II during switching process is always from 0 V to $\pm V_{dc}$ or $\pm 2V_{dc}$, whereas in Technique-I the inverter voltage changes from 0 V to $\pm V_{dc}$ and from $\pm V_{dc}$ to $\pm 2V_{dc}$.

Fig. 20 shows a comparison between the system efficiency using the proposed two PWM techniques. It is cleared that the efficiency of the system controlled by Technique-II is slightly higher than that obtained by using Technique-I when the modulation index is less than 0.5 ($0 < M_I \leq 0.5$) since the high frequency switches is only two in technique-II, whereas technique-I uses four switches operate at high frequency. The difference in efficiency is not high due to the small current flowing in the switches. However, the difference in efficiency of both technique is noticeable when the modulation index is higher than 0.5 ($M_I > 0.5$) due to the high current flowing in the switches. It is cleared that the efficiency of the system controlled by Technique-I is higher than that obtained by using Technique-II when the modulation index is higher than 0.5 ($M_I > 0.5$), although Technique-II uses only two high frequency switches. This is because the reduction in switching loss in Technique-II due to less number of used high frequency switches is less than the increase in switching loss caused by the switching at high voltage difference (from 0 V to $2V_{dc}$) in addition to the losses due to increased harmonics. Based on the experimental results of the efficiency and THD in the single-phase five-level inverter system, using PWM technique-II is better than using PWM technique-I if the modulation index is ($0.0 < M_I \leq 0.5$), whereas using PWM technique-I is better than using PWM technique-II if the modulation index is ($M_I > 0.5$).

IX. CONCLUSION

This paper has presented two control schemes for controlling a single-phase five-level DC-AC inverter. The inverter THD and efficiency are the key-point in designing the PWM switching techniques. PWM Technique-I uses only four switches operating at switching frequency and the other two switches operating at the fundamental line frequency. PWM technique-II uses only two switches operating at switching frequency, two switches operate at double line frequency, and the others operate at line frequency.

![Fig. 18. Comparison between simulation and experimental results of the inverter Total Harmonic Distortion (THD) using PWM technique-I.](image1)

![Fig. 19. Comparison between simulation and experimental results of the inverter Total Harmonic Distortion (THD) using PWM technique-II.](image2)

![Fig. 20. Efficiency of the system using both PWM techniques.](image3)
The effectiveness of the proposed PWM techniques has been verified theoretically and experimentally using laboratory prototype. Experimental results prove that both techniques have the ability to control the inverter output voltage to follow reference one. Experimental results of THD have shown coincidence with the theoretical results. Inverter efficiency and its output voltage THD varies with the modulation index, depending on the reference output voltage. Technique-II is better whenever the modulation index is \( MI \leq 0.5 \) due to its high efficiency, whereas PWM Technique-I is better whenever the modulation index is \( MI > 0.5 \) due to its high efficiency and low THD.

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REFERENCES


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