Three-Level SEPIC with Improved Efficiency and Balanced Capacitor Voltages

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Abstract

The single-ended primary-inductor converter (SEPIC) has the merits of low input current ripple and output voltage up/down capability. However, the switching devices in the two-level SEPIC have high voltage stresses and high switching losses. To cope with this drawback, this paper proposes a three-level SEPIC, which can use a lower-voltage-rated switch having better switching performance compared to the switch in the two-level SEPIC. The three-level SEPIC can decrease the switch voltage stresses and reduce the switching losses. The converter operation and control method are described. The experimental results for a 500 W prototype converter are discussed. The experimental results show that the three-level SEPIC improves the power efficiency with balanced capacitor voltages compared to the two-level SEPIC.

Key words: Three-level, Single-ended primary-inductor converter (SEPIC), Voltage stress, Switching loss, Output capacitor voltage balancing

I. INTRODUCTION

The single-ended primary-inductor converter (SEPIC) has been utilized for various industry applications due to its low input current ripple [1] and output voltage up/down capability [2]. Unlike the buck-boost converter [3], the SEPIC has a non-inverted output voltage [4]. It uses a series capacitor to isolate the input from the output [5]. Fig. 1 shows the circuit diagram of the conventional two-level SEPIC [1], [6]. The main drawback of the two-level SEPIC is the fact that the switching devices are stressed on the sum of the input voltage $V_i$ and the output voltage $V_o$ [7]. When the output voltage $V_o$ is 400 V, the power switch and the output diode should be rated on 1200 V as $V_i$ may go up to 200 V or even more. As the output voltage increases, the switch voltage stress would be highly increased. This high voltage stress increases the switching losses, eventually decreasing the converter efficiency and deteriorating the converter reliability.

The three-level converters are a well-adapted method for high voltage applications [8], [9]. They use two series-connected capacitors for the total dc-link voltage. Then, the power switches are stressed on half of the total dc-link.
The three-level converters can use a lower-voltage-rated switch having better switching performance compared to the switch rated on the full blocking voltage in the two-level converters. The converter performance including the cost and the power efficiency can be improved compared to the two-level converters. Recently, a three-level isolated SEPIC has been studied in [12]. Unfortunately, the isolated type converter should require two transformers, which increases the manufacturing cost and eventually decreases the converter efficiency. However, up to now, any three-level non-isolated SEPIC has not been suggested and its performance has not been reported.

This paper proposes a three-level SEPIC. Fig. 2 shows the circuit diagram of the three-level SEPIC. The three-level SEPIC can reduce the switch voltage stresses by half compared to the two-level SEPIC. This allows the three-level SEPIC to have lower-voltage-rated switches. The three-level SEPIC improves the power efficiency compared to the two-level SEPIC by reducing the switching losses. The operation of the three-level SEPIC is described in Section II. The control method to regulate the output voltage and the capacitor voltages is presented in Section III. The experimental results for a 500 W prototype converter are discussed in Section IV. The experimental results show that the three-level SEPIC improves the power efficiency with balanced capacitor voltages compared to the two-level SEPIC. The concluding remarks are given in Section V.

II. THREE-LEVEL SEPIC

Fig. 3 shows the circuit diagram of the three-level SEPIC with the reference directions of currents and voltages. The three-level SEPIC has an input inductor \( L_i \), two switches \( S_1 \) and \( S_2 \), two capacitors \( C_1 \) and \( C_2 \), an output inductor \( L_o \), two diodes \( D_1 \) and \( D_2 \), and two output capacitors \( C_{o1} \) and \( C_{o2} \). \( R_{o1} \) and \( R_{o2} \) are the output resistors. \( S_1 \) and \( S_2 \) are the metal-oxide-semiconductor field-effect transistors (MOSFETs).

Fig. 4 shows the operation waveforms of the three-level SEPIC: (a) \( D < 0.5 \) and (b) \( D > 0.5 \).

\( V_i \) is an input voltage. \( V_{o1} \) and \( V_{o2} \) are the voltages of \( C_{o1} \) and \( C_{o2} \) respectively. \( V_{o1} \) and \( V_{o2} \) are the voltages of \( C_{o1} \) and \( C_{o2} \) respectively. \( V_{s1} \) and \( V_{s2} \) are the voltages across \( S_1 \) and \( S_2 \) respectively. \( V_{d1} \) and \( V_{d2} \) are the voltages across \( D_1 \) and \( D_2 \) respectively. \( i_{L_i} \) and \( i_{L_o} \) are the currents of \( L_i \) and \( L_o \) respectively. The midpoint of the output capacitors is connected to the midpoint of the series-connected switches. \( C_{o1} \) and \( C_{o2} \) serve as a capacitive voltage divider to split the output voltage \( V_o \) into two equal voltages \( V_{o1} \) and \( V_{o2} \) \((V_{o1} = V_{o2} = V_o/2)\). \( V_{s1} \) and \( V_{s2} \) follow the half of the input voltage \((V_{s1} = V_{s2} = V_i/2)\).

Fig. 4 shows the operation waveforms of the three-level
SEPIC. $V_{g1}$ and $V_{g2}$ are the gating signals of $S_1$ and $S_2$, respectively. $D_{g1}$ and $D_{g2}$ are the duty cycles of $S_1$ and $S_2$, respectively. If $V_{g1}$ and $V_{g2}$ are identical with an 180° phase difference with respect to one switching period $T_s$, the duty cycle is considered as $D$. When the duty cycle $D$ is less than 0.5, the three-level SEPIC steps down the input voltage, as shown in Fig. 4(a). When the duty cycle $D$ is higher than 0.5, the three-level SEPIC steps up the input voltage, as shown in Fig. 4(b). Fig. 5 shows the circuit diagrams of the three-level SEPIC according to the switches’ states. Depending on the switches’ state, the three-level SEPIC has four operation modes as follows:

**Mode I:** The three-level SEPIC is in this mode only when $D > 0.5$. When $S_1$ and $S_2$ are turned on, $D_{g1}$ and $D_{g2}$ are turned off. The input inductor $L_i$ stores energy from the input voltage $V_i$. The input inductor current $i_{L_i}$ flows through $L_i$, $S_1$, and $S_2$ at the rate of $di_{L_i}/dt = V_i/L_i$. On the other hand, the output inductor current $i_{L_o}$ charges the capacitors $C_1$ and $C_2$. The output inductor current $i_{L_o}$ flows through $C_1$, $S_1$, $S_2$, and $C_2$ at the rate of $di_{L_o}/dt = V_o/L_o$.

**Mode II:** $S_1$ is turned on and $S_2$ is turned off. $D_1$ is turned off and $D_2$ is turned on. The input inductor current $i_{L_i}$ charges the capacitors $C_1$ and $C_2$. The input inductor current $i_{L_i}$ flows through $L_i$, $S_1$, $C_{o1}$, $D_1$, and $C_{o2}$ at the rate of $di_{L_i}/dt = (V_i - V_o)/2L_i$. On the other hand, the output inductor current $i_{L_o}$ charges the capacitors $C_1$ and $C_{o2}$. The output inductor current $i_{L_o}$ flows through $C_1$, $S_1$, $C_o$, and $D_2$ at the rate of $di_{L_o}/dt = (V_i - V_o)/2L_o$.

**Mode III:** $S_1$ is turned off and $S_2$ is turned on. $D_1$ is turned on and $D_2$ is turned off. The input inductor current $i_{L_i}$ charges the capacitors $C_1$ and $C_{o1}$. The input inductor current $i_{L_i}$ flows through $L_i$, $C_1$, $D_1$, and $C_{o1}$ at the rate of $di_{L_i}/dt = (V_i - V_o)/2L_i$. On the other hand, the output inductor current $i_{L_o}$ charges the capacitors $C_2$ and $C_{o2}$. The output inductor current $i_{L_o}$ flows through $D_2$, $C_{o2}$, $S_2$, and $C_2$ at the rate of $di_{L_o}/dt = (V_i - V_o)/2L_o$.

**Mode IV:** The three-level SEPIC is in this mode only when $D < 0.5$. When $S_1$ and $S_2$ are turned off, $D_1$ and $D_2$ are turned on. The input inductor $L_i$ releases its stored energy to the output capacitors $C_{o1}$ and $C_{o2}$, discharging the capacitors $C_1$ and $C_2$. The input inductor current $i_{L_i}$ flows through $L_i$, $C_1$, $D_1$, $C_{o1}$, $C_{o2}$, $D_2$, and $C_2$ at the rate of $di_{L_i}/dt = -V_o/L_i$. On the other hand, the output inductor current $i_{L_o}$ flows through $D_1$, $C_{o1}$, $C_{o2}$, and $D_2$ at the rate of $di_{L_o}/dt = -V_o/L_o$.

When $S_1$ and $D_2$ are turned off, they are stressed on the sum of $V_{c1}$ and $V_{c2}$. When $S_2$ and $D_2$ are turned off, they are stressed on the sum of $V_{c1}$ and $V_{c2}$. By the assumption that $V_{cl} = V_{c1} = V_i/2$ and $V_{cu} = V_{c2} = V_o/2$, the switch voltage stress is $(V_i + V_o)/2$. The switch voltage stress in the three-level SEPIC is reduced by half compared to the switch voltage stress in the two-level SEPIC. This allows the three-level SEPIC to have lower-voltage-rated switches and to reduce the switching losses.
III. SIMULATION VERIFICATIONS

The capacitor voltages should be balanced as \( V_{c1} = V_{c2} = \frac{V_i}{2} \) and \( V_{o1} = V_{o2} = \frac{V_o}{2} \). In practice, the capacitor voltages may be different due to the mismatched capacitances and the mismatched equivalent series resistance [10]. If not balanced, one of the capacitor voltages may be greater than the breakdown voltage of the power switch, which causes severe damage to the power switch [11]. Thus, the capacitor voltage balance control is necessary for the three-level SEPIC.

Fig. 6 shows the control scheme of the three-level SEPIC. Fig. 6(a) shows the control block diagram for regulating the input current and the output voltage. To obtain the relation between the control variables and the duty cycle \( D \), \( Mode I \) and \( Mode II \) are considered for a half switching period \( T_s/2 \). When \( S_1 \) and \( S_2 \) are turned on during \( Mode I \), the input inductor current \( i_{Li} \) increases. The following voltage equation is obtained as

\[
\left( \frac{V_i - V_o}{2} \right) - L_i \frac{di_{Li}}{dt} = 0 .
\]  

Depending on the duty cycle \( D \), the average inductor voltage for \( T_s/2 \) gives the input inductor current variation \( \Delta i_{Li} \) as

\[
V_i \left( DT_s - \frac{T_s}{2} \right) + \left( \frac{V_i - V_o}{2} \right) \left( T_s - DT_s \right) = L_i \Delta i_{Li} .
\]  

By rearranging (3),

\[
\left( \frac{V_i + V_o}{2} \right) D = \frac{V_o}{2} + \frac{L_i \Delta i_{Li}}{T_s} .
\]  

Here, the duty cycle \( D \) is represented as

\[
D = D_n + D_c .
\]  

where a nominal duty cycle \( D_n \) and the controlled duty cycle \( D_c \) are represented as

\[
D_n = \frac{V_o}{V_i + V_o} .
\]
\[ D_t = \frac{2L_s I_{L_s}}{(V_i + V_o)B_s}. \]  

(7)

To regulate the output voltage \( V_o \) to track its voltage reference \( V_o^* \), a proportional-integral (PI)-type voltage controller is used for the controlled duty cycle \( D_c \) as

\[ D_c = k_p V_{o,\text{err}} + k_i \int V_{o,\text{err}} \, dt. \]  

(8)

\[ V_{o,\text{err}} = V_o^* - V_o. \]  

(9)

The voltage error \( V_{o,\text{err}} \) is obtained by comparing the voltage reference \( V_o^* \) to the measured output voltage \( V_o \). \( k_p \) and \( k_i \) are the proportional and integral control gains of the controller, respectively.

Fig. 6(b) shows the control block diagram for balancing the capacitor voltages. The duty cycle \( D_{S1} \) is decided by the voltage controller. On the other hand, the duty cycle \( D_{S2} \) is decided by adding additional duty cycles \( D_{C1} \) and \( D_{C2} \) with the duty cycle \( D_{S1} \) whose phase is shifted by 180°. The duty cycle \( D_{C1} \) is

\[ D_{C1} = k_p V_{C1,\text{err}} + k_i \int V_{C1,\text{err}} \, dt. \]  

(10)

\[ V_{C1,\text{err}} = V_{c2} - V_{c1}. \]  

(11)

where \( k_p \) and \( k_i \) are the proportional and integral gains of the controller, respectively. \( V_{C1,\text{err}} \) is the voltage error between \( V_{c2} \) and \( V_{c1} \). The duty cycle \( D_{C2} \) is

\[ D_{C2} = k_p V_{C2,\text{err}} + k_i \int V_{C2,\text{err}} \, dt. \]  

(12)

\[ V_{C2,\text{err}} = V_{o2} - V_{o1}. \]  

(13)

where \( k_p \) and \( k_i \) are the proportional and integral gains of the controller, respectively. \( V_{C2,\text{err}} \) is the voltage error between \( V_{o2} \) and \( V_{o1} \). By the suggested capacitor voltage balancing control, the capacitor voltages can be balanced. As the duty cycle \( D_{S2} \) is different from \( D_{S1} \), the load currents flowing through \( R_{o1} \) and \( R_{o2} \) would be slightly different while the capacitor voltages are balanced.

IV. EXPERIMENTAL RESULTS

To evaluate the performance of the three-level SEPIC, a 500 W prototype converter has been built and tested. Table I shows the electrical specification of the prototype converter. The two-level SEPIC has been also designed for the performance comparison with the three-level SEPIC. Table II shows the main component parameters of the two converters. In order to select the inductances of \( L_1 \) and \( L_o \), the inductor ripple current is taken into account. Generally, the inductance is proportional to the voltage induced across each inductor. Also, the duty cycle should be considered with the inductor ripple current. As the inductor ripple current increases, the minimum inductance could be decreased with respect to the duty cycle for the voltage across the inductor. On the other hand, in order to select the capacitances of \( C_1 \), \( C_2 \), \( C_{o1} \), and \( C_{o2} \), the capacitors are primarily designed for reducing capacitor voltage ripples. As the capacitor voltage ripples are reduced, the capacitances of the capacitor should be increased. The film capacitors, as non-polarized capacitors, could be used for \( C_1 \) and \( C_2 \) because they follow the half of the input voltage. Meanwhile, the electrolytic capacitors, as polarized capacitors, could be used for \( C_{o1} \) and \( C_{o2} \) because they supply electric power to the output load, serving as a capacitive voltage divider to split the output voltage into two equal voltages \( V_{o1} \) and \( V_{o2} \).
Fig. 7 shows the experimental waveforms of the two-level SEPIC: (a) switch voltage $V_{S1}$ and the diode voltages $V_{D1}$ for $D = 0.41$ and (b) switch voltage $V_{S2}$ and the diode voltages $V_{D2}$ for $D = 0.60$.

The two-level SEPIC uses 11N80C3 (Infineon) for $S_1$ whose voltage rating is 800 V. It uses RHRP15120 (Fairchild) for $D_1$ whose voltage rating is 1200 V. Fig. 7(a) shows the switch voltage $V_{S1}$ and the diode voltage $V_{D1}$ when the duty cycle $D$ is 0.41 for $V_i = 200$ V. The balanced resistive load is used. The output voltage $V_o$ is 140 V for $R_{o1} = R_{o2} = 39 \, \Omega$. The switch voltage stress is calculated as 340 V theoretically. However, the peak switch voltage stress with the voltage spike is measured as 550 V. When the switch is turned off, the output diode cannot be turned off instantly. Because of the reverse-recovery process of the diode, it causes large reverse-recovery current, which causes a voltage spike across the power switch. This kind of switching operation is called as hard-switching operation [13]. Fig. 7(b) shows the switch voltage $V_{S2}$ and the diode voltage $V_{D2}$ when the duty cycle $D$ is 0.60 for $V_i = 200$ V. The output voltage $V_o$ is 300 V for $R_{o1} = R_{o2} = 180 \, \Omega$. The switch voltage stress is calculated as 500 V theoretically. However, as shown in Fig. 7(b), due to its hard-switching operation, the peak switch voltage stress with the voltage spike is measured as 700 V.

Fig. 8 shows the experimental waveforms of the two-level SEPIC for a 500 W output power. The two-level SEPIC uses 11N80C3 (Infineon) for $S_i$ whose voltage rating is 800 V. It uses RHRP15120 (Fairchild) for $D_i$ whose voltage rating is 1200 V. Fig. 8(a) shows the switch voltage $V_{S1}$ and the diode voltages $V_{D1}$ and $V_{D2}$ for $D = 0.41$ and (b) switch voltages $V_{S1}$ and $V_{S2}$ and the diode voltages $V_{D1}$ and $V_{D2}$ for $D = 0.60$.

Fig. 9 shows the experimental waveforms of the three-level SEPIC: (a) inductor current waveforms of the two-level SEPIC and (b) inductor current waveforms of the three-level SEPIC.

Fig. 9. Experimental waveforms of the two-level SEPIC and the three-level SEPIC: (a) inductor current waveforms of the two-level SEPIC and (b) inductor current waveforms of the three-level SEPIC.

Fig. 7 shows the experimental waveforms of the two-level SEPIC for a 500 W output power. The two-level SEPIC uses 11N80C3 (Infineon) for $S_i$ whose voltage rating is 800 V. It uses RHRP15120 (Fairchild) for $D_i$ whose voltage rating is 1200 V. Fig. 7(a) shows the switch voltage $V_{S1}$ and the diode voltage $V_{D1}$ when the duty cycle $D$ is 0.41 for $V_i = 200$ V. The balanced resistive load is used. The output voltage $V_o$ is 140 V for $R_{o1} = R_{o2} = 39 \, \Omega$. The switch voltage stress is calculated as 340 V theoretically. However, the peak switch voltage stress with the voltage spike is measured as 550 V. When the switch is turned off, the output diode cannot be turned off instantly. Because of the reverse-recovery process of the diode, it causes large reverse-recovery current, which causes a voltage spike across the power switch. This kind of switching operation is called as hard-switching operation [13]. Fig. 7(b) shows the switch voltage $V_{S2}$ and the diode voltage $V_{D2}$ when the duty cycle $D$ is 0.60 for $V_i = 200$ V. The output voltage $V_o$ is 300 V for $R_{o1} = R_{o2} = 180 \, \Omega$. The switch voltage stress is calculated as 500 V theoretically. However, as shown in Fig. 7(b), due to its hard-switching operation, the peak switch voltage stress with the voltage spike is measured as 700 V.

Fig. 8 shows the experimental waveforms of the three-level SEPIC for a 500 W output power. The three-level SEPIC uses FQA24N50 (Fairchild) for $S_i$ and $S_2$ whose voltage rating is 500 V. It uses FES8JT (Vishay) for $D_1$ and $D_2$ whose voltage...
rating is 600 V. Fig. 8(a) shows the switch voltages \(V_{S1}\) and \(V_{S2}\) and the diode voltages \(V_{D1}\) and \(V_{D2}\) when the duty cycle \(D\) is 0.41 for \(V_i = 200\) V. The output voltage \(V_o\) is 140 V for \(R_{o1} = R_{o2} = 39\) Ω. The voltage stress of the switching devices is calculated as 170 V, which is half of the voltage stress of the switching devices in the two-level SEPIC. However, due to its hard-switching operation, the peak switch voltage stress with the voltage spike is measured as 300 V. Fig. 8(b) shows the switch voltages \(V_{S1}\) and \(V_{S2}\) and the diode voltages \(V_{D1}\) and \(V_{D2}\) when the duty cycle \(D\) is 0.60 for \(V_i = 200\) V. The output voltage \(V_o\) is 300 V for \(R_{o1} = R_{o2} = 180\) Ω. The voltage stress of the switching devices is calculated as 250 V. However, as shown in Fig. 8(b), due to its hard-switching operation, the peak switch voltage stress with the voltage spike is measured as 300 V.

Fig. 9 shows the experimental waveforms of the two-level SEPIC and the three-level SEPIC when \(V_i = 200\) V for \(D = 0.60\) and a 500 W output power. Fig. 9(a) shows the inductor current waveforms of the two-level SEPIC. The current ripple is observed as 2.0 A. The current ripple frequency is the same as the switching frequency of 50 kHz. Fig. 9(b) shows the inductor current waveforms of the three-level SEPIC. The current ripple is 1.0 A, which is two times lower than the current ripple of the two-level SEPIC. The current ripple frequency is 100 kHz, which is two times higher than the switching frequency of 50 kHz.

Fig. 10 shows the experimental waveforms of the three-level SEPIC and the three-level SEPIC when \(V_i = 200\) V for \(D = 0.60\) and a 500 W output power. Fig. 10(a) shows the capacitor voltages when the output voltage is regulated as \(V_o = 300\) V without the capacitor voltage balance control. The three-level SEPIC has operated for \(V_i = 200\) V, \(R_{o1} = 86\) Ω, and \(R_{o2} = 94\) Ω. As the output voltage \(V_o\) is regulated as \(V_o = 300\) V, not only the output capacitor voltages \(V_{o1}\) and \(V_{o2}\) but also the capacitor voltage \(V_{c1}\) and \(V_{c2}\) are unbalanced as \(V_{o1} = 120\) V, \(V_{o2} = 180\) V, \(V_{c1} = 160\) V, and \(V_{c2} = 40\) V due to the mismatched series-connected output resistances. Fig. 10(b) shows the capacitor voltages when the output voltage is regulated as \(V_o = 300\) V with the capacitor voltage balance control. The three-level SEPIC has operated for \(V_i = 200\) V, \(R_{o1} = 86\) Ω, and \(R_{o2} = 94\) Ω. As the output voltage \(V_o\) is regulated as \(V_o = 300\) V, the output capacitor voltages \(V_{o1}\) and \(V_{o2}\) are balanced as \(V_{o1} = 150\) V and \(V_{o2} = 150\) V. Also, the capacitor voltages \(V_{c1}\) and \(V_{c2}\) are balanced as \(V_{c1} = 150\) V and \(V_{c2} = 150\) V.
balanced as \( V_{c1} = 100 \) V and \( V_{c2} = 100 \) V by the suggested capacitor voltage control.

Fig. 11 shows the measured power efficiencies of the two-level SEPIC and the three-level SEPIC, respectively. The power efficiencies have been measured for different output power levels when the output voltage is controlled as \( V_o = 140 \) V and \( V_o = 300 \) V, respectively, for \( V_i = 200 \) V. Fig. 11(a) shows the measured power efficiencies when the output voltage is 140 V for a 500 W output power. The two-level SEPIC has the efficiency of 91.6 %. On the other hand, the three-level SEPIC achieves the efficiency of 93.4 %. The three-level SEPIC improves the efficiency by 1.8 % compared to the two-level SEPIC when the output voltage is 140 V from \( V_i = 200 \) V. Fig. 11(b) shows the measured power efficiencies when the output voltage is 300 V for a 500 W output power. The two-level SEPIC has the efficiency of 95.0 %. Meanwhile, the three-level SEPIC achieves the efficiency of 94.0 %. The three-level SEPIC improves the power efficiency by 1.0 % compared to the two-level SEPIC when the output voltage is 300 V from \( V_i = 200 \) V for a 500 W output power. Fig. 12(a) and (b) show the photographs of the two-level and three-level SEPICs, respectively. The converters are controlled by a single-chip micro-controller, dsPIC30F2020 (Microchip). A voltage divider with an operational amplifier has been designed for sensing the capacitor voltages. In order to generate phase-shifted pulse-width modulation (PWM) signal, a power supply PWM module in dsPIC30F2020 has been utilized.

V. CONCLUSIONS

This paper has proposed a three-level SEPIC to overcome the drawback of the conventional two-level SEPIC. Compared to the two-level SEPIC, the three-level SEPIC has lower switch voltage stresses. The three-level SEPIC reduces the switch voltage stress by half compared to the two-level SEPIC. This allows the three-level SEPIC to use lower-voltage-rated switches and to reduce the switching losses. The converter operation has been described. The converter control has been also presented for regulating the output voltage with the capacitor voltage balance control. The experimental results for a 500 W prototype converter have been discussed. The experimental results have shown that the three-level SEPIC improves the power efficiency with balanced capacitor voltages compared to the two-level SEPIC. The three-level SEPIC improves the efficiency by 1.8 % when it steps down the input voltage of 200 V into the output voltage of 140 V for a 500 W output power. The three-level SEPIC improves the efficiency by 1.0 % when it steps up the input voltage of 200 V into the output voltage of 300 V for a 500 W output power. The proposed three-level SEPIC is expected to be utilize for the photovoltaic and fuel-cell power generations.

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