Design of a High-precision Constant Current AC-DC Converter with Inductance Compensation

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Abstract

A primary-side regulation AC-DC converter operating in PFM (Pulse frequency modulation) mode with high precision output current is designed, which applies a novel inductance compensation technique to improve the precision of output current, diminishing the bad impact of the big tolerance of the transformer primary side inductance in the same batch. In this paper, the output current is regulated by the OSC charging current, which is controlled by CC (constant current) controller. Meanwhile, for different primary inductors, the inductance compensation module adjusts the OSC charging current finely to improve the accuracy of output current. The operation principle and design of CC controller and inductance compensation module are analyzed and illustrated herein. The control chip is implemented based on TSMC 0.35\(\mu\)m 5V/40V BCD process, and a 12V/1.1A prototype has been built to prove the proposed control method. The deviation of output current is within ±3% and the variation of output current is less than 1% when the inductance of primary windings vary by 10%.

Key words: AC-DC converter, primary-side regulation, PFM, constant current, inductance compensation

I. INTRODUCTION

The flyback AC-DC converter with PSR (primary-side regulation) structure is widely used in many power supply applications, including LED drivers, chargers for portable electronic equipment and off-line power supply adapters [1] [2] [3]. It has the advantages of simplicity and cost-effectiveness. Compared with the conventional secondary feedback converters, the topology of primary-side regulation has no demand of the optical coupler and the precise voltage source [4] [5], reducing the volume and the cost [6] [7]. Besides, the PSR structure has a good system reliability. Nevertheless, for the PSR converter, high demands are required on the performance of the transformer. For CC controller, PFM is a common mode for adjustment due to its high efficiency and feasibility [8]. The CC output accuracy of the PSR constant current AC-DC converter is easily affected by the primary inductance of transformer. However, the inductance of the primary windings in the same batch has a tolerance of ±10%. Thus, for the CC converter, an inductance compensation function should be employed in the circuit, to reduce the variation of output current caused by the difference on the primary inductance.

A primary side inductance compensation circuit is proposed in [9]. The compensation module adjusts the input power, which is influenced by the primary inductance, keeping it constant. But, it only accomplishes the theoretical analysis. Another compensation technology for inductance tolerance is illustrated in [10]. A target time is set to indicate how long the primary current reaches a predetermined current limit. The real ramp time before the primary current stops increasing, and is compared to this target time and the error signal is used to adjust the switching frequency and pulse width, maintaining constant output current. But this compensation circuit has a complex structure. In addition, a primary inductance correction circuit is introduced in [11]. The compensation current is generated based on the output current sampled and injected into the OSC for regulating switching frequency, to correct the output power change caused by inductance tolerance. However, the output accuracy is constrained by the sampling precision.

Above all, a PSR High-precision constant current AC-DC converter, operating in PFM mode and adopting inductance compensation method, is presented in this paper. The detailed operation principle and design of constant current and compensation are illustrated in Section II. The experimental results based on a prototype will be given in Section III. Section VI will make a conclusion of the proposed design.
II. DESIGN OF PSR AC-DC CONTROLLER CHIP

A. System Review

The system diagram of the PSR constant current AC-DC flyback converter with the proposed control chip is shown in Fig. 1 [12], comprised of bridge rectifier BD, EMI filter, RCD clamp circuit, freewheel diode $D_0$ and $D_1$, capacitor $C_0$ and $C_a$, transformer, power switch $M_1$, primary current sensing resistor $R_{CS}$, pull-up resistor $R_1$ and pull-down resistor $R_2$, control IC. For this control chip, INV pin is used to detect the information of output voltage through auxiliary winding, CS pin is to detect the primary side current, and GATE pin, to drive the power switch.

The block diagram of control IC, shown in Fig. 1, mainly consists of Sampling trigger module, OSC (Oscillator) module, PFM generator, Inductance compensation module, CS peak controller and Gate driver module. The switching frequency is generated by OSC module and in proportional to the charging current. The sampling trigger module contains the sampler and the Demag module, which is a demagnetization time detector. The information of the output voltage is sampled from the auxiliary winding cycle by cycle, and inputted to the CC controller, then the CC controller regulates the frequency of OSC, making the PFM generator create a modulated pulse for driving the power switch. The CS peak controller is used to maintain the primary peak current constant. The inductance compensation module, including control circuit, charge pump, voltage to current (V/I) converter and compensation starting delay circuit, is applied to compensate the loss of the output current accuracy owing to the different inductance of the transformer primary windings in the same batch.

B. Design of Constant Current Modules

PFM mode is employed to achieve constant current output. In switch power circuit, the output power can be expressed as:

$$P_o = \frac{1}{2} \eta \cdot L_p \cdot F_s \cdot I_{pp}^2$$

where $\eta$ is the transformer conversion efficiency, $L_p$ is primary inductance, $F_s$ is switching frequency and $I_{pp}$ is primary peak current.

In the PSR controller shown in Fig. 1, the relationship between the voltage of INV pin and the output voltage $V_o$ is:

$$V_o = \frac{R_1 + R_2}{N \cdot R_1} \cdot V_{INV}$$ \hspace{1cm} (2)

In eq. (2), $R_1$ is the pull-up resistance and $R_2$ is the pull-down resistance, $V_{INV}$ is the voltage sampled from INV pin. $N$ is turn’s ratio of auxiliary and secondary windings. Based on eq. (1) and eq. (2), the output current $I_o$ can be derived as:

$$I_o = \frac{1}{2} \eta \cdot L_p \cdot F_s \cdot N \cdot \frac{R_2}{R_1 + R_2} \cdot \frac{V_{INV}}{V_o}$$ \hspace{1cm} (3)

On the basis of the analysis above, OSC charging current is adjusted based on the sampled voltage $V_{INV}$ (OSC charging current is proportional to $V_{INV}$) and OSC charging current is proportional to $F_s$ to keep the ratio of $F_s$ and $V_{INV}$ constant. However, the output current precision is influenced by the conversion efficiency of transformer $\eta$, as it may vary slightly under different input voltage and load.
For the converter operating in PFM mode, if the load is extremely light (the output voltage is extremely low), the switching frequency $F_S$ would drop to a very small value, causing the $V_{INV}$ sampling speed quite slowly as a result of $V_{INV}$ being sampled cycle by cycle. When the load jumps from the light to the heavy, the controller couldn’t handle the load step rapidly and the output current would decrease instantly. It would take too long response time for the output to recover constant. In order to overcome this shortcoming of PFM mode, it is necessary to determine a minimum value of switching frequency. However, it will increase the power dissipation under light load.

The CC controller is shown in Fig. 2, in which $EA$ is an error amplifier, $INV1$ is an inverter and $COMP1$ is a current comparator. The connection between the CC controller and the inductance compensation module is also can be seen in Fig. 2.

In Fig. 2, $en1$ is the active-low enable signal for inductance compensation module. $I_{OSC}$, the OSC charging current, can be expressed as:

$$I_{OSC} = \begin{cases} \frac{V_{INV}}{R_i} - I_{OSCadj} & (I_1 \geq I_2) \\ I_2 & (I_1 < I_2) \end{cases} \quad (4)$$

$I_{OSCadj}$ is the fine adjusting current from inductance compensation module, which helps to improve the accuracy of output current. $I_1$ is proportional to $V_{INV}$, $I_2$ is a constant value.

![Fig. 2. CC (constant current) Controller.](image)

For the circuit in Fig. 2, if $I_1$, the current controlled by $V_{INV}$ and inductance compensation module, is less than $I_2$, $I_{OSC}$ equals to $I_2$ due to the current comparator, determining the minimum frequency under CC mode. If $I_1$ is larger than $I_2$, $I_{OSC}$ is controlled linearly by $V_{INV}$ with the scale factor $1/R_i$ and regulated slightly by inductance compensation module.

**C. Design of Inductance Compensation Circuit**

For the flyback converters produced in the same batch, the inductance of the transformer magnetizing inductors has a tolerance of about 10%, which leads to the inconsistent output current from these converters. It can be explained based on the equation of $I_e$, eq. (3). The magnetizing inductor of flyback converter is the primary inductor of transformer. Hence, the inductance compensation module is needed, in order to acquire constant output current unrelated to primary inductance $L_p$.

The process of CC regulation is illustrated in Fig. 3. It is seen that when the system begin to start up, the compensation module doesn’t work at first. The CC controller enter the operating state and the output current rises to an initial value, which is a little larger than the target value. At this moment, the primary inductance has a bearing on output current and the accuracy can be easily influenced. Until the state of output current has just been steady, the inductance compensation module works and then makes the output current drop to the target value. Now, the accuracy of output current is immune to the unstable primary inductance and maintained at a constant level.

![Fig. 3. The process of CC regulation.](image)

It is known that $L_p$ is difficult to be measured directly, thus $L_p$ can be calculated based on demagnetization time $T_D$ and primary peak current $I_{pp}$:

$$L_p = \frac{V_{pp}}{\sqrt{\eta \cdot I_{pp} \cdot T_D}} \quad (5)$$

where $n$ is the turn’s ratio of primary and secondary windings. According to eq. (1) and eq. (5), the output current equation can be inferred as follows:

$$I_o = \frac{1}{2} \sqrt{\eta \cdot n \cdot I_{pp} \cdot T_D \cdot T_S} \quad (6)$$

From the analysis above, the primary peak current $I_{pp}$ is fixed. So, if the product of demagnetization time $T_D$ and switching frequency $F_S$ is constant, it can be noticed from eq. (6) that the output current would keep constant and is unconcerned to $L_p$. Besides, comparing the transformer conversion efficiency $\eta$ in eq. (3) and eq. (6), it’s obvious that the variation of $\eta$ has relatively less influence on the output current if the CC regulation is based on eq. (6). Then the higher output current precision can be achieved.

In order to obtain an unchanged product of $T_D$ and $F_S$, the inductance compensation module detects the demagnetization time $T_D$ and compares it with the half switching period, $1/2T_S$. If $T_D$ is shorter than $1/2T_S$, the compensation module would
decrease $I_{\text{oscadj}}$ to increase $I_{\text{osc}}$, making the switching period shorter. On the contrary, if $T_0$ longer than 1/2$T_s$, the compensation module increases $I_{\text{oscadj}}$ to decrease $I_{\text{osc}}$, then the switching period becomes longer. After several switching periods for adjusting, $T_0$ is forced to be equal to 1/2$T_s$, namely, the product of $T_D$ and $F_s$ remains a constant value 1/2.

The inductance compensation circuit includes four main parts: control circuit, charge pump, V/I converter and compensation starting delay circuit. Each part plays an important role in the regulation process. These circuits are then about to be analyzed in detail.

1) Control circuit: The control circuit is the core part of the inductance compensation module, offers the control signal based on $T_D$ and 1/2$T_s$, just as shown in Fig. 4. COMP2 is a comparator and FF1 is a rising-edge triggered D flip-flop. $V_{\text{demag}}$ is the demagnetization signal from the Demag module and CLK is the output signal of OSC.

![Fig. 4. Design implementation of control circuit.](image)

The length of $T_D$ and 1/2$T_s$ should be converted to the corresponding voltage in order to detect them conveniently. Based on the current equation of capacitance:

$$I = C \frac{dV_C}{dt} \quad (7)$$

The voltage on the capacitor can be calculated as eq. (8) if the current $I$ is constant.

$$V_C = \frac{1}{C} \int I dt \quad (8)$$

In Fig. 4, $C_2 = 2C_1$. Thus, the voltage of $V_{C1}$ and $V_{C2}$ represents the length of $T_D$ and 1/2$T_s$. The working process of the control circuit is shown in Fig. 5.

As is seen in Fig. 5, two switching periods compose one working period. During the first switching period, $M_{10}$ is turned on by the logic circuit and $C_1$ is charged by $I_5$ at the rising edge of the demagnetization signal $V_{\text{demag}}$, when the demagnetization occurs. $M_{10}$ is turned off when the demagnetization is over and voltage $V_{C1}$ on capacitor $C_1$ stays constant. In the whole second switching period, $M_{11}$ is turned on and $C_2$ is charged by $I_5$. At the end, the voltage $V_{C1}$ on capacitor $C_1$ is compared with the voltage $V_{C2}$ on capacitor $C_2$, the result is then stored in D flip-flop and stays unchanged until the end of another two switching periods. In Fig. 5, $ctl$ is at low level when $V_{C1} > V_{C2}$. In contrast, if $V_{C1} < V_{C2}$, $ctl$ would be switched to high.

![Fig. 5. Working process of the control circuit.](image)

After one working period, in order not to affect the next comparison, the charge on $C_1$ and $C_2$ should be released immediately. In Fig. 5, $C_1$ and $C_2$ is discharged quickly through $M_{12}$ and $M_{13}$ when $V_t$ at high level before the demagnetization in the first switching period.

2) Charge pump circuit: The charge pump is shown in Fig. 6. According to the output result of the control circuit, the charge pump offers the control voltage $V_{\text{ctl}}$, which will be converted to OSC charging current adjusting current, to improve or reduce the charging current of OSC, for adjusting the switching frequency.

![Fig. 6. Design implementation of charge pump circuit.](image)

In Fig. 6, en1, from the CC controller, and en2, from the compensation starting delay circuit, are the active-low enable
signals for the compensation module. Signal $ctl$, the output of the control circuit, is the input signal and $V_{ctl}$ is the output voltage.

Supposing signal $ctl$ is at low level, $M_{18}$ is at ON state and $M_{19}$ is at OFF. The capacitor $C_3$ is charged by $I_4$ through current mirror. At this moment, the voltage $V_{ctl}$ is ramping up slowly. On the contrary, if $ctl$ at high level, $M_{18}$ is at OFF state and $M_{19}$ is at ON, the charge on $C_3$ is released by $I_4$ through current mirror, so $V_{ctl}$ begins to ramp down.

3) Voltage to current converter: The voltage to current (V/I) converter receives the control voltage from the charge pump and regulates the switching frequency by adjusting the OSC charging current, for the sake of a constant product of $T_D$ and $F_S$. Fig. 7 shows the converter circuit.

![Fig. 7. Design implementation of V/I converter.](image)

In the circuit in Fig. 7, $M_{27}$ and $R_6$ is identical to $M_{28}$ and $R_7$, converting $V_{ctl}$ to the current which is in proportion to $V_{ctl}$. Then, this current is transported to the output $I_{OSCadj}$ by current mirror. $I_{OSCadj}$ makes a fine regulation to $I_{OSC}$, obliging the switching frequency to vary with the demagnetization time. An unchanged product of $T_D$ and $F_S$ can be achieved after several working periods. Thus, a constant output current unrelated to primary inductance is obtained.

![Fig. 8. Key waveform of inductance compensation adjustment](image)

Six working periods of the compensation adjustment is shown in Fig. 8, the level of $ctl$ is decided by $T_D$ and $1/2T_S$. It is seen that $I_{OSCadj}$ increases with $V_{ctl}$ in one working period while $ctl$ is low and decreases while $ctl$ is high. The switching frequency can be regulated well by the adjusting circuit.

4) Compensation starting delay circuit: According to the analysis above, the inductance compensation adjustment is realized by reducing the OSC charging current moderately. Hence, in the start-up process of system, the compensation module may decrease the switching current, making the CC controller start slowly. In order to avoid this problem, the operation of the compensation circuit should be delayed until after the system has completely started.

![Fig. 9. Compensation starting delay circuit.](image)

The compensation starting delay circuit is adopted in the inductance compensation module. Its function is to lock the compensation circuit at the beginning of the system’s start-up and enables it when the output current becomes relatively stable. As is shown in Fig. 9, the circuit consists of a 4096 times frequency divider, a NOR gate, a falling-edge triggered D flip-flop $FF_2$ and a rising-edge triggered D flip-flop $FF_3$.

![Fig. 10. Working process of the starting delay circuit.](image)

In Fig. 9, the output $Q$ of the two D flip-flops are both reset to low level by a transient low level pulse when the circuit just powered on. Since the start-up frequency is about 14kHz, a pulse with a period of about 292ms can be obtained by dividing the frequency of CLK 4096 times. This signal is about to switch after 146ms from the system just starts. The two D flip-flops detect the rising or falling edge at this moment. Signal $en2$ switches to high after having detected the edge. Thus, the starting delay circuit doesn’t unlock the compensation function until 146ms later after start-up of system. The working process of the starting delay circuit can be seen in Fig. 10.

III. EXPERIMENTAL RESULTS

A. Layout Design of the Control IC

The proposed AC-DC converter is implemented in TSMC 0.35μm 5V/40V BCD process and the area is 904×920μm²,
as is shown in Fig. 11. The key modules are marked in the photograph. The designed PCB is shown in the Fig. 12, its size is about 5.9cm × 3.4cm.

**Fig. 11.** Photograph of the implemented chip.

**Fig. 12.** Photograph of the fabricated PCB.

### B. Test Results of Proposed Control Chip

As is seen in Fig. 1, the proposed AC-DC controller adopts PSR flyback topology. The key components and parameters of the circuit are listed in Table I.

The related waveforms of the circuit operating in CC mode are shown in Fig. 13. The input voltage is 90Vac/60Hz and 264Vac/50Hz and the output voltage is 7V and 10V. The first curve from top to bottom is output current, $I_o$; the second is the sampled voltage from auxiliary winding, $V_{INV}$; the third is the sampled voltage across the primary current sense resistor, $V_{CS}$.

According to Fig. 13, the maximum of $V_{CS}$ is fixed at 900mV, which indicates the primary peak current $I_{PP}$ is an unchanged value. The demagnetization time $T_D$ is nearly equal to the half of the switching period $T_S$. The output current in every figure is almost 1.1A, of which the deviation is less than ±3%. The test results are accordant with analysis based on eq. (6).

**TABLE I**

<table>
<thead>
<tr>
<th>Components</th>
<th>Symbol</th>
<th>Value or Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Brige rectifier</td>
<td>BD</td>
<td>1N4007</td>
</tr>
<tr>
<td>Primary-side inductance</td>
<td>$L_p$</td>
<td>0.8mH</td>
</tr>
<tr>
<td>Transformer core</td>
<td>T</td>
<td>EE22</td>
</tr>
<tr>
<td>Power switch</td>
<td>$M_1$</td>
<td>2N60</td>
</tr>
<tr>
<td>Transformer turn’s ratio</td>
<td>$N_P/N_S/N_{AUX}$</td>
<td>72/11/32</td>
</tr>
<tr>
<td>Pull-up resistor</td>
<td>$R_1$</td>
<td>30KΩ</td>
</tr>
<tr>
<td>Pull-down resistor</td>
<td>$R_2$</td>
<td>3.7KΩ</td>
</tr>
<tr>
<td>Auxiliary-side Freewheel diode</td>
<td>$D_1$</td>
<td>FR107</td>
</tr>
<tr>
<td>Primary current sense resistor</td>
<td>$R_{CS}$</td>
<td>1.05Ω</td>
</tr>
<tr>
<td>Output capacitor</td>
<td>$C_o$</td>
<td>900μF</td>
</tr>
<tr>
<td>Secondary-side Freewheel diode</td>
<td>$D_o$</td>
<td>SR3100</td>
</tr>
</tbody>
</table>

(a) 90Vac & 60Hz-$V_{in}$, 7V-$V_{o}$ measured waveforms

(b) 90Vac & 60Hz-$V_{in}$, 10V-$V_{o}$ measured waveforms

(c) 264Vac & 50Hz-$V_{in}$, 7V-$V_{o}$ measured waveforms
Fig. 13. Test results of output current with different load voltages.
Top trace: \( I_o \); second trace: \( V_{INV} \); third trace: \( V_{CS} \).

Fig. 14 depicts the curves of output current \( I_o \) when output load voltage varies from 5 to 12V, under 90Vac/60Hz-input and 264Vac/50Hz-input respectively. It is shown that the output current keeps constant at about 1.1A and the deviation is less than ±3%.

Fig. 15 shows the output current with different primary inductors when the input voltage is 220Vac/50Hz.

Fig. 16. Measured efficiency versus \( V_o \) under 90Vac & 60Hz-input and 264Vac & 50Hz-input

The system efficiency in CC mode is tested and depicted in Fig. 16 when input voltage is 90V/60Hz and 264V/50Hz, respectively. Obviously, the efficiency under low input voltage is lower than that under high input voltage. The minimum of the system efficiency can reach about 80%.

Above all, the performance of the proposed chip is listed in table 2. It can be seen that the accuracy of output current is very high and adopting the proposed inductance compensation technology has received good effect.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
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<tbody>
<tr>
<td>AC input voltage</td>
<td>90–264 Vac</td>
</tr>
<tr>
<td>AC input frequency</td>
<td>47–63Hz</td>
</tr>
<tr>
<td>Output current</td>
<td>1.1A</td>
</tr>
<tr>
<td>Max output voltage</td>
<td>12V</td>
</tr>
<tr>
<td>Max switching frequency</td>
<td>55kHz</td>
</tr>
<tr>
<td>System efficiency</td>
<td>&gt;80%</td>
</tr>
<tr>
<td>Deviation of output current</td>
<td>&lt;±3%</td>
</tr>
<tr>
<td>Variation of output current</td>
<td>&lt;±1%</td>
</tr>
</tbody>
</table>

According to the curve drawn in Fig. 15, the primary inductance varies by over 10%, but the output current can keep constant and the variation is within ±1%. As there exists the deviation in the conversion efficiency of the transformers used, the variation of the output current is inevitable. It indicates that the inductance compensation module does reduce the negative impact of the tolerance of primary inductance.

IV. CONCLUSIONS

A PSR constant current AC-DC converter operating in PFM mode with inductance compensation is designed and implemented. The primary-side regulation structure omits the optical-coupler and the precise voltage source to reduce the size and cost of the converter. The inductance compensation function eliminates the influence caused by the inductance tolerance of the primary windings and a constant output current can be acquired. In order to verify the proposed compensation technology, a control chip adopting this
method is fabricated in TSMC 0.35μm 5V/40V BCD process and a 12V/1.1A prototype has been built. The experiment results show that the deviation of output current is within ±3%, the variation of output current is less than 1% when the variation of the primary inductance is ±10%.

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