Analysis, Design and Implementation of a High Performance Rectifier

Chien-Ming Wang†, Chin-Wang Tao*, and Yu-Hao Lai*

†,*Department of Electrical Engineering, National Ilan University, Yilan, Taiwan

Abstract

A high performance rectifier is introduced in this paper. The proposed rectifier combines the conventional pulse-width-modulation technique, soft commutation technique and instantaneous average line current control technique to promote the circuit performance. The voltage stresses of main switches in it are lower than them in conventional rectifier topologies. Moreover, the conduction losses of switches in it are certainly lower than them in conventional rectifier topologies because the power current flow path when the main switches are turned on includes two main power semiconductors and the power current flow path when the main switches are turned off includes one main power semiconductor for it. It also adopts a ZCS-PWM auxiliary circuit to realize ZCS function for power semiconductors. Thus, the problem of switching losses and EMI can be improved. In the control strategy, its controller uses average current control mode to accomplish fixed-frequency current control with stability and low distortion. A prototype has been implemented in laboratory to verify circuit theory.

Key words: Rectifier, Soft switching, Pulse-width modulation

I. INTRODUCTION

DC power supply is an essential electric power source of various electronic products. Using a full-bridge diode rectifier with a large filter capacitor as the front-end rectification to get dc output voltage is the conventional method. However, this method will encounter excessively large peak input current and high harmonic distortion. Its input power factor is lower about 0.5-0.6. It does not meet the IEC61000-3-2 limits. Thus, the electronic product designers must research how to reduce input current harmonics and enhance input power factor for their dc power supplies. Inserting a power factor correction (PFC) circuit into the dc power supply is the most popular method.

In various active power factor correctors, the boost power factor corrector is the most general circuit shown in Fig. 1(a) [1]-[7]. However, its conduction losses are larger because the power current flow paths in it always include three main power semiconductors. Moreover, the commutation losses of main power semiconductors in it are also larger because its main power semiconductors are operated under hard-switching.

In order to improve this problem, several power factor correctors with low conduction losses are proposed [11]-[14]. They are basic two-switch bridgeless PFC boost rectifier shown in Fig. 1(b) [11]-[13] and totem pole bridgeless PFC boost rectifier shown Fig. 1(c) [14]. Their conduction losses are certainly lower than previous topologies because the power current flow paths in them only include two main power semiconductors. For improving their commutation losses, several soft-switching topologies for them have been proposed [15]-[19]. In the previous topologies, the voltage stresses of main active power switches in them equal output voltage $V_o$. However, because the cost of semiconductors is dependent on the rated operation voltage, reducing voltage stress of semiconductors is more important subject.

For more reducing conduction losses and commutation losses, a high performance rectifier is proposed in this paper shown in Fig. 1(d). The conduction losses in it are certainly lower than them in previous topologies because the power current flow path when the main switches are turned on only includes two main power semiconductors and the power current flow path when the main switches are turned off only includes one main power semiconductor for it. Moreover, it uses a ZCS auxiliary circuit to realize ZCS function for the power semiconductors in it. Thus, its commutation losses can be improved. Its efficiency will be higher than one of previous mentioned topologies. Moreover, the voltage stress of main
active power switches in it is equal to $V_o/2$ and is lower than one of previous mentioned topologies. Thus, its main circuit cost can be decreased. The comparisons of the number of semiconductors in power current flow path and voltage stress on main semiconductors are shown in table I and II, respectively.

Thus, low voltage stresses, low switching losses, low conduction losses and low EMI noise can be achieved in it. In the control strategy, its controller uses average current-mode control to accomplish fixed-frequency current control with stability and low distortion. Thus, it has well dynamic characteristic. Its behavior is described by seven transition states during one switching period in the positive half-line period. A design strategy is built and a physical system of 1kW proposed rectifier is realized to assess the system performance.

### TABLE I

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<tr>
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<th>Main switches</th>
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<tr>
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<td>Basic two-switch bridgeless PFC boost rectifier</td>
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<td>Proposed high performance rectifier</td>
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### TABLE II

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### II. PRINCIPLE OF PROPOSED HIGH PERFORMANCE RECTIFIER

#### A. Circuit Description

The power stage diagram of proposed rectifier is shown in Fig. 1(d). It composes of a low conduction losses bridgeless PFC boost rectifier with low voltage stress and a ZCS auxiliary circuit. The low conduction losses bridgeless PFC boost rectifier with low voltage stress is operated in continuous conduction mode. Moreover, it composes of an input inductor $L_{in}$, two main switches $S_{m1}$ and $S_{m2}$, two main diodes $D_1$ and $D_2$, two output capacitors $C_{o1}$ and $C_{o2}$. It performs power factor correction function.

The ZCS auxiliary circuit is composed of two diodes $D_{a1}$, $D_{a2}$, two resonant inductors $L_{r1}$, $L_{r2}$, two resonant capacitors $C_{r1}$, $C_{r2}$, and two switches $S_{a1}$, $S_{a2}$, which are rated for a small power when compared to the output power. It is used to realize ZCS function for all power semiconductors in the proposed rectifier.

#### B. Principle of Operation

The drive signals of both the main power switches ($S_{m1}$ and $S_{m2}$) in the proposed rectifier are shown in Fig. 2(b). They are the same. Thus, both the main switches are simultaneously turned on and off. Thus, the control circuit can be simplified.

Fig. 1 (a) Conventional PFC boost rectifier [1], (b) Basic two-switch bridgeless PFC boost rectifier [11], (c) Totem pole bridgeless PFC boost rectifier [14], (d) Proposed high performance rectifier.
Moreover, the commercial PFC IC can be employed. The control circuit cost can be reduced. In the positive half cycle of input line voltage, the current flows through the switch $S_{m1}$ and the anti-parallel diode of switch $S_{m2}$ when both the switches $S_{m1}$ and $S_{m2}$ are turned on. The power current flow path is changed to flow through diode $D_1$ when both the switches $S_{m1}$ and $S_{m2}$ are turned off. Similarly, in the negative half cycle of input line voltage, the current flows through the switch $S_{m2}$ and the anti-parallel diode of switch $S_{m1}$ when both the switches $S_{m1}$ and $S_{m2}$ are turned on. The power current flow path is changed to flow through diode $D_2$ when both the switches $S_{m1}$ and $S_{m2}$ are turned off. Thus, the lower conduction losses are achieved because the power current flow path when both the switches $S_{m1}$ and $S_{m2}$ are turned on only includes two power semiconductors and the power current flow path when both the switches $S_{m1}$ and $S_{m2}$ are turned off includes one power semiconductor. Moreover, the proposed rectifier is dual boost rectifier topology. One boost rectifier which composes of $L_{in}$, $S_{m1}$, the anti-parallel diode of switch $S_{m2}$, $D_1$ and $C_{o1}$ is operated in the positive half cycle of input line voltage. Another boost rectifier which composes of $L_{in}$, $S_{m2}$, the anti-parallel diode of switch $S_{m1}$, $D_2$ and $C_{o2}$ is operated in the negative half cycle of input line voltage. It is symmetrical topology. The voltages across $C_{o1}$ and $C_{o2}$ of the proposed rectifier without the additional balance circuit are almost the same. Thus, the voltages across $C_{o1}$ and $C_{o2}$ are almost equal to $V_o/2$. The voltage stress across the main power switches are almost equal to $V_o/2$.

![Fig. 2 (a) Topological states for operation mode. (b) Gate signals of main switches.](image)

C. State of Operation of the Proposed High Performance Rectifier

In proposed rectifier circuit, the circuit operation in positive half cycle of input line voltage is the same as one in negative half cycle of input line voltage. To simplify the analysis, the circuit operation in positive half cycle of input line voltage is only described in this paper. Because the proposed rectifier is focused on higher power demand, it is operated in CCM. The operation time interval of ZCS auxiliary circuit is a short time interval compared with one switching period. Thus, the input current $i_{in}$ and output voltage $V_o$ can be assumed as constant values $I_{ink}$ and $V_o$ in $k$th switching period, respectively. In addition, the following assumptions are made during one switching cycle.

1. The input voltage in $k$th switching period is constant and equals $V_{ink}$.
2. $V_{c1}(t)$ equals zero and $i_{r1}(t)$ equals $I_{ink}$.

Based on these assumptions, circuit operations in one switching cycle can be divided seven states. The seven dynamic equivalent circuits and the ideal relevant waveforms of the proposed rectifier during one switching period are shown in Fig. 3 and Fig. 4, respectively.

**STATE 1:** $[t_{k0}, t_{k1}]$, Fig. 3(a).

Before state 1, $S_{m1}$ and $S_{m2}$ maintain turn-off state. The energy stored inductors $L_{in}$ and $L_{r1}$ is delivered to capacitor $C_{o1}$ through $D_1$. This state starts when the gates of $S_{m1}$ and $S_{m2}$ are triggered. $S_{m1}$ is turned on under ZCS. Although $S_{m2}$ is triggered, it is not turned on. The resonant inductor $L_{r1}$ discharges linearly by output voltage $V_o$. The resonant current $i_{r1}(t)$ decreases from $I_{ink}$ to zero. The state finishes when $i_{r1}(t)$ reaches zero and diode $D_1$ is naturally turned off.

**STATE 2:** $[t_{k1}, t_{k2}]$, Fig. 3(b).
The inductor \( L_{in} \) is charged by \( V_{in} \) in this time. The other semiconductors maintain turn-off state.

**STATE 3:** \([t_{k2}, t_{k3}]\), Fig. 3(c).

When \( S_{k3} \) is turned on under ZCS, the resonance behavior of \( C_{r1} \) and \( L_{r1} \) starts and this state also starts. The resonant path is through \( V_{ol}, L_{r1}, C_{r1}, \) and \( S_{k1} \). When \( i_{L_{r1}}(t) \) increases and then decreases when it arrives its peak value, \( v_{c_{r1}}(t) \) also increases. When \( i_{L_{r1}}(t) \) drop to zero, the state ceases.

**STATE 4:** \([t_{k3}, t_{k4}]\), Fig. 3(d).

During this state, the resonance behavior of \( C_{r1} \) and \( L_{r1} \) is hold. However, the resonant path is changed through \( V_{ol}, L_{r1}, C_{r1}, D_{a1}, S_{m1}, \) and the anti-parallel diode of \( S_{m2} \). Although the resonant current can flow through the anti-parallel diode of \( S_{m2} \), the resonant current still only flows through \( S_{m1} \) and anti-parallel diode of \( S_{m1} \). This is because the voltage drop of \( S_{m1} \) and anti-parallel diode of \( S_{m2} \) counterbalances the voltage drop of the anti-parallel diode of \( S_{m1} \), which makes low impedance current path through \( S_{m1} \) and anti-parallel diode of \( S_{m2} \). Moreover, based on Kirchhoff’s current law, \( i_{e_{r1}} = i_{m1} - i_{L_{r1}} \). Because \( i_{e_{r1}} \) is less than \( i_{m1} \), \( i_{m1} \) is positive, no current flows \( S_{m1} \) and the current flows anti-parallel diode of \( S_{m2} \). \( v_{c_{r1}}(t) \) decreases and \( i_{L_{r1}}(t) \) increases. This state ceases when \( i_{L_{r1}}(t) \) rises to \( I_{in} \).

**STATE 5:** \([t_{k4}, t_{k5}]\), Fig. 3(e).

The previous resonance operation is still maintained in this state. However, the resonant current flows through \( V_{ol}, L_{r1}, C_{r1}, \) and the anti-parallel diode of \( S_{m1} \). Because the resonant current \( i_{e_{r1}} \) is larger than the input current \( i_{m1} \). The anti-parallel diode of \( S_{m2} \) is reverse bias and it is naturally turned off. Thus, no current flows through \( S_{m1}, S_{m2}, S_{o1} \). It is the best time to turn \( S_{m1}, S_{m2}, S_{o1} \) off under zero-current condition. Thus, \( S_{m1}, S_{m2}, S_{o1} \) are
turned off at \( t = t_{lo} \). \( v_{Cr1}(t) \) continuously decreases. \( i_{Lr1}(t) \) increases and then decreases when it arrives its peak value. This state ceases when \( i_{Lr1}(t) \) drop to \( I_{in} \) again.

**STATE 6**: \([t_k, t_{lo}]\), Fig. 3(f).

The resonant capacitor \( C_r \) is discharged through \( D_{al}, C_{r1}, L_{r1}, \) and \( V_{out} \) in this state. Therefore, \( v_{Cr1}(t) \) decreases linearly toward zero. This state ceases when \( v_{Cr1}(t) \) drop to zero again.

**STATE 7**: \([t_{lo}, t_{s2}]\), Fig. 3(g).

In this state, the input inductor \( L_{in} \) is charged by \( V_{in} \). This state is kept until \( S_{al} \) is turned on under zero-current condition again.

After state 7, the circuit operation is returned to the first state. \( v_{Cr1}(t) \) equals zero and \( i_{Lr1}(t) \) also equals \( I_{in} \). Thus, the assumption previously is valid.

![Fig. 4 The waveforms diagram of proposed high performance rectifier under the kth switching period in positive half cycle of input line voltage.](image)

**D. Output Characteristics**

Because the proposed rectifier is operated steady-state, the inductor voltage must satisfy voltage-second rule under one switching period. Thus,

\[
V_{out} \approx \left[ (1 - D) - \frac{\Delta t_3}{T_s} - \frac{\Delta t_1}{T_s} - \frac{\Delta t_2}{T_s} \right] \frac{V_s}{2}
\] (1)

where

\[
\Delta t_1 = t_{s1} - t_{s2} = \frac{\pi}{\omega_L}
\] (2)

\[
\Delta t_2 = t_{s2} - t_{s1} = \frac{1}{\omega_L} \arcsin \left( \frac{I_{in} Z_{in}}{V_s} \right)
\] (3)

\[
\Delta t_3 = t_{s3} - t_{s4} = \frac{\pi}{\omega_L} - 2 \Delta t_4
\]

\[
Z_r = \frac{L_r}{C_r}
\]

\[
\omega_L = \frac{1}{\sqrt{L_r C_r}}
\]

The voltage conversion ratio \( (M) \) can be given as equation (7).

\[
M(D) = V_s V_{in, rms} \leq \frac{2\sqrt{2}}{(1 - D) - 1 - \frac{1}{2\pi} \sin^2 \left( \sqrt{2} I_{in, rms} Z_{in} \right) f_s f_e}
\]

Moreover, the voltage conversion ratios of the other topologies shown in Fig. 1 are identical and equal \( \sqrt{2}/(1 - D) \). The voltage conversion ratio of proposed rectifier without ZCS auxiliary circuit is \( 2\sqrt{2}/(1 - D) \). Thus, the proposed rectifier has a voltage doubler characteristic compared with them. In addition, the voltage conversion ratio of proposed rectifier with ZCS auxiliary circuit is shown in equation (7). It shows that \( f_s/f_e \) will influence the voltage conversion ratio. Because the ZCS auxiliary circuit is an auxiliary role, the smaller \( f_s/f_e \) is recommended for reducing the influence of \( f_s/f_e \).

**E. Commutation Analysis**

From the operation analysis of stage 5, the constraint of following inequalities should be satisfied for achieving soft commutation in the proposed high performance rectifier.

\[
\frac{V_s}{Z_s} > I_{in, peak}
\]

Moreover, the turn-on time interval \( \Delta t_{on, S_{al}, 2} \) of the switch \( S_{al, 2} \) must be less than the minimum conduction time.

\[
\Delta t_{on, S_{al, 2}} \leq (1 - D_{min}) T_s,
\]

where \( D_{min} \) is minimum duty-cycle.

The time interval \( \Delta t_{on, S_{al, 2}} \) is governed by

\[
\Delta t_{on, S_{al, 2}} = \Delta t_1 + \Delta t_2 = \frac{\pi}{\omega_L} + \frac{1}{\omega_L} \sin^2 \left( \frac{I_{in} Z_{in}}{V_s} \right)
\]

**III. CONTROL STRATEGY**

The functional block diagram of the controller of the proposed high performance rectifier is shown in Fig. 5(a). Moreover, the detail control circuit of the proposed high performance rectifier is shown in Fig. 5(b). The controller can be divided into two sections which are main power factor correction part and soft-switching control logic part. The main power factor correction part adopts the average current-mode control method to correct the power factor. This paper uses the commercial PFC control IC UC3854 which is produced by Texas Instruments Company performs the basic power factor
correction function. The function block diagram of the IC UC3854 is shown in Fig. 5(a). For obtaining close unity power factor, the UC3854 senses the synchronous line input voltage from the transformer T. Moreover, it uses a multiplier/divider to combine some necessary signals which include the feedforward synchronous line input voltage, the root-mean-square (rms) line input voltage, and the output feedback error voltage to generate the current reference of the current error amplifier. For achieving the average current-mode control function, the current error amplifier in the UC3854 uses the current reference and the output current signal of Hall-effect sensor to generate the error current. Then, the error current signal is inputted the pulse-width modulator. The pulse-width modulator uses a comparator to compare the error current with the sawtooth waveform which is a constant frequency signal to generate the main power factor correction PWM control signal which is the signal in pin 16 of the UC3854.

For getting the soft-switching control signals, the main power factor correction PWM control signal then is inputted to the soft-switching control logic part which composes of a monostable multivibrator, tow comparators, some logic gates and four drive circuits. From Fig. 5(b), the two comparators are used to determine the operational cycle of input line voltage. First, the main power factor correction PWM control signal triggers the monostable multivibrator (IC CD4047) by the negative-edge trigger mode. The monostable multivibrator then outputs a constant pulse width which is the control signal of the auxiliary switches. The constant pulse width is distributed to the auxiliary switches $S_{a1}$ and $S_{a2}$ according to the output signals of the two comparators. If the proposed rectifier operates in the positive half cycle of input line voltage, the constant pulse width signal is transmitted to drive $S_{a1}$. On the other hand, it is transmitted to drive $S_{a2}$. Secondly, about the generation method of the control signals of the main power switches ($S_{m1}$ and $S_{m2}$), the main switches must be held on state during the auxiliary switches are turned on according to the previous main power circuit analysis. The main power factor correction PWM control signal must be synthesized with the constant pulse width signal by OR gate to generate the new power factor correction PWM control signal. Because both the main switches ($S_{m1}$ and $S_{m2}$) are simultaneously turned on and off according to previous main power circuit analysis, the new power factor correction PWM control signal is direct triggered the two power switches.

![Functional block diagram and circuit diagram of the proposed high performance rectifier](image-url)

**Fig. 5 (a)** The functional block diagram of controller of the proposed high performance rectifier. (b) Detail circuit of the proposed high performance rectifier controller.

## IV. DESIGN CONSIDERATIONS AND EXPERIMENTAL RESULTS

A high performance rectifier is designed and realized as an example. Its specifications are listed below:

- **Input voltage:** $v_{in}(t)=155\sin(2\pi*60t)$
- **Output voltage:** $V_o=400V$
- **Maximum output power:** $P_{out,max}=1000W$
- **Switching frequency:** $f_s=40kHz$

The implemented power stage circuit of proposed rectifier is shown in Fig. 5(a). It is focused on higher power demand. Therefore, it is operated under continuous conduction mode (CCM). Its design procedure is described as follows with previously described circuit characteristics.

1. **Consideration on input current ripple and selection of the input inductor $L_i$.**

   When the input line voltage is maximum, the duty ratio $D$ is minimum and can be calculated as follow according to the
conversion ratio of the conventional boost converter.

\[ D_{\text{max}} = (1 - \frac{V_{\text{out,peak}}}{V_o/2}) = 0.225 \]  

(10)

The input ripple current is also maximum value in this time. It can be denoted as follows.

\[ \Delta I_{\text{in}} = \frac{V_{\text{in,peak}}}{L_o} D_{\text{max}} T_i \]  

(11)

The input ripple current is selected as 10% input maximum current. Thus,

\[ \Delta I_{\text{in,max}} = 0.1 \times \sqrt{2} \times \frac{P_{\text{max}}}{V_{\text{in,peak}}} = 1.286 \text{A} \]  

(12)

Thus,

\[ L_o = \frac{V_{\text{in,peak}}}{\Delta I_{\text{in,max}}} D_{\text{max}} T_i = 678 \text{μH} \]  

(13)

Thus, \( L_o = 680 \text{μH} \) is selected.

2) Selection of output capacitor.

The selection of output capacitor is dependent on the switching frequency ripple current, the second harmonic ripple current, the output ripple voltage and the hold-up time which is defined as the time required for the output voltage to remain within regulation after the ac input voltage is removed. However, the hold-up time often dominates the other factors in output capacitor selection. The output capacitor \( C_o \) will select according to hold-up requirements. Thus,

\[ C_o \geq \frac{2 P_{\text{max}} \Delta t}{V_o^2 - V_{\text{in,peak}}^2} \]  

(14)

where \( \Delta t \) is hold-up time, \( P_{\text{max}} \) is the maximum output power, \( V_o \) is the output voltage and \( V_{\text{in,peak}} \) is the minimum output voltage that the load can normal operate.

In this case, \( \Delta t = 34 \text{ms} \), \( P_{o}=1000\text{W}, V_o=400\text{V}, V_{\text{in,peak}}=300\text{V}. \)

Thus, \( C_o \) is 971μF. \( C_o = 940 \text{ μF} \) is selected.

3) Selection of the Resonant Parameters.

Using the specifications data, the maximum input current can be obtained as follows when the output power is rated maximum power.

\[ I_{\text{in,max}} = \sqrt{\frac{2 P_{\text{max}}}{V_{\text{in,peak}}}} = 12.86 \text{A} \]  

(15)

Thus, the peak input current is as follows.

\[ I_{\text{in,peak}} = I_{\text{in,max}} + \frac{\Delta I_{\text{in,max}}}{2} = 13.5 \text{A} \]  

(16)

The equation (7) shows that the voltage conversion ratio is relative to the parameters \( D, f_c/f_o \). The more the value of \( f_c/f_o \) is lower, the more the influence of ZCS switching cell is lower. Thus, it is recommended that the value of \( f_c/f_o \) is lower than 0.3. In this case, \( f_c/f_o = 0.1 \) is selected. Thus,

\[ \omega_o = \frac{1}{\sqrt{L_o C_o}} = 2\pi f_o = 20\pi f_o = 2.513 \times 10^4 \text{ rad/s}. \]  

(17)

The inequality in (8) should be satisfied in order to ensure that the main power switch turns on and off under ZCS. Hence,

\[ Z_o = \frac{L_o}{\sqrt{C_o}} \leq \frac{V_o}{2 I_{\text{in,peak}}} = 14.81 \text{Ω} \]  

(18)

Thus, expression (18) divided by (17) leads to

\[ L_o \leq \frac{V_o}{4\pi f_o I_{\text{in,peak}}} = 5.893 \times 10^{-9} \text{H} \]  

(19)

\( L_o = 4\mu\text{H} \) is selected for clearing the phenomenon of zero-current-switching. Substituting \( L_o = 4\mu\text{H} \) into (17), \( C_o = 39.59\text{nF} \) can be obtained, and \( C_o = 47\text{nF} \) is selected.

4) Selection of the main power switches and diodes.

From the circuit operation analysis, the maximum current through the main switches \( (S_{a1}, S_{a2}) \) and the main diodes \( (D_1, D_2) \) and the maximum voltages across them can be calculated as follows.

\[ i_{\text{D1,1, max}} = i_{\text{D2,2, max}} = I_{\text{in,max}} = \sqrt{\frac{2 P_{\text{max}}}{V_{\text{in,peak}}}} = 12.86 \text{A} \]  

(20)

\[ v_{\text{D1,1, max}} = v_{\text{D2,2, max}} = V_o / 2 = 200 \text{V} \]  

(21)

\[ i_{\text{D1,1, max}} = i_{\text{D2,2, max}} = I_o = \frac{P_{\text{max}}}{V_o} = 2.5 \text{A} \]  

(22)

\[ v_{\text{D1,1, max}} = v_{\text{D2,2, max}} = V_o = 400 \text{V} \]  

(23)

5) Selection of auxiliary power switches and diodes.

The maximum current through the auxiliary switch \( S_o \) and the maximum voltage across it can also be obtained as follow from the circuit operation.

\[ i_{\text{D1,1, max}} = i_{\text{D2,2, max}} = I_{\text{r, peak}} = \frac{V_o / 2}{Z_o} = 13.5 \text{A} \]  

(24)

\[ v_{\text{D1,1, max}} = v_{\text{D2,2, max}} = V_o / 2 = 200 \text{V} \]  

(25)

In addition, the maximum current through the auxiliary diodes \( D_1, D_2 \) and the maximum voltage across them can also be obtained as follow from the circuit operation.

\[ i_{\text{D1,1, max}} = i_{\text{D2,2, max}} = I_{\text{r, peak}} = \frac{V_o / 2}{Z_o} = 13.5 \text{A} \]  

(26)

\[ v_{\text{D1,1, max}} = v_{\text{D2,2, max}} = V_o = 400 \text{V} \]  

(27)

Thus, in hardware realization, MOSFET’s IRFP 264 and DSEP30-06A are selected as the power switches and diodes. UC3854 is selected as the controller. The circuit parameters of UC3854 controller can be decided according to [20]. Fig. 6(a) illustrates the experimental platform for this work. The waveforms of the input voltage and current are shown in Fig. 6(b), in which the waveforms of the input voltage and current are almost in phase and the measured power factor is over 0.99. The high power factor has been achieved. The commutation phenomenon in the main switches \( S_{a1} \) and \( S_{a2} \), the auxiliary switches \( S_o \), and \( S_{a2} \), and the main diodes \( D_1 \) and \( D_2 \) are
measured in Fig. 6(c), Fig. 6(d), and Fig. 7(a), respectively. The experimental results shown in Fig. 6(c), Fig. 6(d), and Fig. 7(a) demonstrate that ZCS are achieved for these active switches (Sm1, Sm2, and Sa). It should be noticed that the main diodes D1 and D2 were also softly commutated under ZCS. Therefore, the switching losses for the main switches and the main diodes are practically zero. Moreover, the voltage stresses of active power switches are equal to \( V_{o}/2 = 200\) V according to the experimental results of Fig. 6 and Fig. 7. Comparing with the other topologies with soft-switching technique [15]-[19], they are equal to a half of the voltage stresses of active power switches in the topologies [15]-[19]. The feature of lower voltage stress on active power switches in the proposed rectifier has been achieved and verified.

![Experimental platform](image)

The measured power factor curves versus output power with different input voltage and versus input voltage with different output power are shown in Fig. 7(b). The power factors are over 0.9 in all condition. Thus, it demonstrates that high power factor is achieved. The measured efficiency curves versus output power with different topologies are shown Fig. 7(c). Because the traditional topologies shown in Fig. 1(a), Fig. 1(b) and Fig. 1(c) are operated in hard-switching, the efficiencies of the topologies with soft-switching technique are the proposed rectifier and the topologies in [16]-[17] is higher than the efficiencies of the traditional topologies shown in Fig. 1(a), Fig. 1(b) and Fig. 1(c). It can be verified from the experimental results in Fig. 7(c). Moreover, the conduction losses in proposed rectifier are less than them in [16]-[17] which are the topologies with soft-switching technique. The efficiency of the proposed rectifier is higher than the efficiency of the topologies in [16]-[17]. It can also be verified form the experimental result in Fig. 7(c). The transient waveforms of the output voltage and current during load change are shown in Fig. 7(d). It demonstrates that the influence of load changing on the output voltage is small. Thus, the dynamic characteristic of proposed rectifier is good.

![Waveforms](image)

V. CONCLUSIONS

A high performance rectifier is proposed in this paper. A prototype circuit of the proposed rectifier has been implemented. The proposed rectifier has many characteristics as follow.
1) The main switches Sm1, Sm2, D1, and D2 can achieve ZCS.
2) The main switches Sm1 and Sm2 have lower voltage stresses compared with the other boost rectifiers.
3) The proposed rectifier uses the ZCS auxiliary circuit to get soft-switching function.
4) The proposed rectifier is regulated by the conventional
PWM technique at constant frequency. Thus, it combines the advantages of the PWM and soft-switching techniques.

5) High power efficiency about 95.5% is acquired under the rated power of 1000W.

![Fig. 7 (a) Commutation in the auxiliary switches $S_{a1}$ and $S_{a2}$ under 1000W output power rating. $V_{DSa1}, V_{DSa2}$: 100V/div; $I_{DSa1}, I_{DSa2}$: 10A/div, time: 4μs/div](image)

(b) Power Factor according to output power.

(c) Experimental efficiency of proposed ZCS bridgeless PFC boost rectifier compared with the other topologies.

(d) Transient waveforms of the output voltage and current during load change ($V_o$: 250 V/div; $I_o$: 1A/div, time: 20 ms/div).

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REFERENCES


Chien-Ming Wang was born in Miaoli, Taiwan, R.O.C., in 1966. He received the M.S. degree in electrical engineering from National Taiwan Ocean University, Keelung, in 1995, and the Ph.D. degree in electronic engineering from National Taiwan University of Science and Technology, Taipei, in 2000. He is currently a Professor with the Department of Electrical Engineering, National Ilan University, I-Lan, Taiwan, where he has been a Faculty Member since 2005. He has been engaged in research and teaching in the areas of power electronics, electronic circuit design, and control system.

Chin-Wang Tao received the B.S. degree in electrical engineering from National Tsing Hua University, Hsinchu, Taiwan, R.O.C., in 1984, and the M.S. and Ph.D. degrees in electrical engineering from New Mexico State University, Las Cruces, in 1989 and 1992, respectively. He is currently a Professor with the Department of Electrical Engineering, National Ilan University, I-Lan, Taiwan. His research interests are on the fuzzy neural systems including fuzzy control systems and fuzzy neural image processing. Dr. Tao is an Associate Editor of the IEEE Transactions on Systems, Man, and Cybernetics.

Yu-Hao Lai was born in Changhua, Taiwan, R.O.C. in 1987. He received the M.S. degree in electrical engineering from National Ilan University, Taiwan, in 2012. His current research interests include switch mode converters.