Singular Value Decomposition based Space Vector Modulation to Reduce the Output Common-mode Voltage of Direct Matrix Converters

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Abstract

Large magnitude common-mode voltage (CMV) and its variation dv/dt have an adverse effect on motor drives that will lead to early winding failure and bearing deterioration. For matrix converters, the switch states that connect each output line to a different input phase result in the lowest CMV among all valid switch states. To reduce the output CMV for matrix converters, this paper presents a new space vector modulation (SVM) strategy by utilizing these switch states. By this mean, not only the peak value but also the root mean square of the CMV is decreased dramatically. In comparison with the conventional SVM methods this strategy has a similar computation overhead. Experiment results are shown to validate the effectiveness of the proposed modulation method.

Key words: Common-mode Voltage, Matrix Converters, Singular Value Decomposition, Space Vector Modulation

I. INTRODUCTION

For the past decades, the matrix converter (MC) continues to be an attractive topology for three-phase AC-AC power conversion [1]–[3]. The main reason for this interest lies in the potential advantages of MCs, such as bi-directional power flow, flexible input power factor, and no large energy storage elements. The superior features brings great benefits for wind energy conversion systems, adjustable speed drives and other applications, thus motivates extensive attentions on MCs.

The modulation strategy is one of the pivotal factors that have a significant impact on the performance of a MC. The existing modulation methods for MCs are intrinsically based on the well-known pulse-width modulation [4]. As a result of the PWM switching pattern, MCs generate staircase-like high frequency common-mode voltage (CMV) waveforms. Large magnitude CMV and its high frequency variation dv/dt, unfortunately, are claimed to be one of the important reasons for early winding failure and motor bearing deterioration [5].

To mitigate the CMV of MCs, several methods have been reported in literature. A common-mode canceler that acts similarly as an active filter is proposed to alleviate CMVs [6]. Dual structure converters are applied to both direct- and indirect-MC-fed open-end winding drives to further reduce or eliminate the CMV output [7]–[10]. However, these methods need additional devices which increase the costs and thus are not considered in this paper.

Another method to suppress the CMV issue is to modify the modulation strategies. Two active vectors with opposite directions [11]–[14] or three nearest-state vectors [13], [14] are used to replace those zero vectors with high CMVs. These methods use more than five vectors, and thus increase the switching count. Besides, modulation strategies using three nearest vectors can be only applied in applications of high voltage transfer ratio (VTR) above 0.667. In order to reduce the switching count, Hong-Hee Lee et al. proposed strategies using two vectors with 120° phase shift [15], [16]. However, this strategy can be only applied in applications of low VTR below 0.5.
The switch states which connect each input line to a different output phase and have zero output CMV are not well explored in the aforementioned modulations. The difficulty of including them in the modulation process might account for the fact that they are not widely used. Ren Vargas et al. added a term in the quality function of their predictive current model to control the CMV [17]–[20]. Yet, this method has a high computational overhead. Yugo Tadano et al. tried to use these switch states, but at the cost of a complex switch pattern selection [21], [22].

This paper presents a CMV-reduced modulation for direct matrix converters based on the singular value decomposition (SVD) on all valid switch states [23]–[25]. Relationships between different switch states are first found, so that the OSSs are introduced in by equivalent substitution. With part of CMV waveforms being suppressed to zero, the proposed method decreases both the peak value and the root mean square (RMS) of the CMV. Because of the similarity, the proposed method has almost the same computation overhead in comparison with the conventional space vector modulation (SVM) method. The proposed method can also synthesize the reference variables without the measurement on the output currents, thus save the costs.

Another contribution of this paper lies in that it provides an insight to the switch states of MCs by applying the SVD to the space vector representation of the transfer functions. The SVD results in a set of submatrices for all valid switch states. Since the geometrical meanings of SVD can help reveal the fundamental characteristics on how each switch state transforms a column vector between two different coordinates, this treatment offers a new basis for interpreting the modulation process.

II. SINGULAR VALUE DECOMPOSITION BASED SPACE VECTOR MODULATION

A. Matrix Converter System Model

The three-phase direct MC consists of a nine-switch array, as shown in Fig. 1. If the switches are modeled as ideal switching functions, the voltage relationship between both sides of the MC can be expressed as follows [23]–[26],

\[
V_s = \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} S_{aa} & S_{ab} & S_{ac} \\ S_{ba} & S_{bb} & S_{bc} \\ S_{ca} & S_{cb} & S_{cc} \end{bmatrix} \begin{bmatrix} v_A \\ v_B \\ v_C \end{bmatrix} = SV, \tag{1}
\]

where transfer function S is the switch state matrix (SSM), representing the connection of the MC array. Similarly, the current relationship can be formulated as \( I = S' I_s \), where the superscript “T” means the transposition operation. Typically, the converter connects both the voltage source and current source. Consequently, only 27 switch state patterns are valid for safe operations.

In the existing modulation methods, the SSMs are consid-

![Fig. 1. Three-phase direct matrix converter Configuration.](image)

ered together with the input voltages and output currents to get the resultant vectors before the duty cycles are determined. However, even if the inputs are ideal, either the amplitudes or the angles of the resultant voltage or current vectors are fluctuating [27]. This brings difficulties in the determination of the duty cycles. Actually, the SSMs preserve the intrinsic characteristics of MCs, regardless the variation of the inputs. Therefore, this paper separately considers the SSMs and the system inputs, and starts from the voltage relationship. In order to simplify the analysis, Eq. (1) is transformed into its space vector representation, i.e. \( V_{αβγ} = T^{-1} V_{αβγ} \), from the abc coordinates into the α-β reference frame by

\[
T = \frac{2}{3} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \tag{2}
\]

No zero sequence current flows in three-phase-three-wire systems. Therefore, ignoring the zero-sequence component, the voltage relationship can be expressed in matrix form [23],

\[
\begin{bmatrix} v_{αr} \\ v_{βr} \end{bmatrix} = \begin{bmatrix} S_{αα} & S_{αβ} \\ S_{βα} & S_{ββ} \end{bmatrix} \begin{bmatrix} v_{αr} \\ v_{βr} \end{bmatrix} = S_{αβ} v_{αr} + v_{βr}, \tag{3}
\]

where \( S_{αβ} \) is the space vector form of the transfer matrix S in Eq. (1), and \( xy \) represents the input phases that connect to the output phases. For example, when the output phases ABC connect to the input phases in the order of abb, \( S_{αβγ} \) can be written as \( S_{αβγ} \). Here the input and the output voltage space vectors are \( \bar{v}_α = V_α + jV_β \), \( \bar{v}_β = V_α + jV_β \) respectively.

B. Singular Value Decomposition of the Space Vector Transfer Matrix for All Valid Switch States

To reveal how the transfer function matrix transforms the input voltage column vector to the output one, \( S_{αβγ} \) in Eq. (3) is factorized by the SVD method into the multiplication of

\[
s_{αβ} = U_{αβ} S_{αβ} V_{αβ}^{-1} \tag{4}
\]

where \( U_{αβ} \) and \( V_{αβ} \) are the left and right singular vectors. The SVD factorization yields the singular values (SV) of the transfer matrix S. The singular values reveal the magnitude of the voltage relationship and the singular vectors show the direction of the transfer from one space vector to another.

The singular values are determined by the square (RMS) of the CMV. Because of the similarity, the OSSs are introduced in by equivalent substitution. With part of the CMV waveforms being suppressed to zero, the proposed method decreases both the peak value and the root mean square (RMS) of the CMV. Because of the similarity, the proposed method has almost the same computation overhead in comparison with the conventional space vector modulation (SVM) method. The proposed method can also synthesize the reference variables without the measurement on the output currents, thus save the costs.
three matrices, representing as $S_{xyz} = U \cdot D \cdot V^T$, where $U$ and $V$ are unitary matrices and $D$ is a diagonal matrix with $a_d$ and $a_b$ being the diagonal elements. These SSMs can be categorized into three types according to their SVD results, as listed in Table I.

1) **Type I Switch States**: These switch states have zero output line voltages and thus result in zero voltage space vectors by connecting all outputs to one same input phase. For this type SSMs, the diagonal elements in the matrices $D$s are all zero.

2) **Type II Switch States**: These switch states connect two and only two output phases to one input phase, having a common feature that all of their factorized $U$s and $V$s are rotation matrices. It is important to point out that the rotation angles of $Us$ and $Vs$ are determined only by the switch states and are independent of the input voltages. If these rotation matrices are represented by their corresponding rotation vectors with the same effective angles, two hexagons with unit radius at the input and the output sides respectively, can be obtained in Fig. 2. Both hexagons are actually different from those in the traditional SVM, where the resultant voltage or current space vectors of the switch states together with the input voltages or output currents have fixed angles but variable amplitudes [27]. Type II switch states are also summarized in Table II, with the rotation angles of their decomposed $Us$ and $Vs$ matching the positions of their equivalent rotation vectors in both hexagons of Fig. 2.

3) **Type III Switch States**: Corresponding to the traditional SVM, the last six switch states listed in Table I result in rotating output voltage space vectors with fixed amplitudes since unitary matrices are isometry, but with variable angles depending on both the switch states and the inputs. The matrices $D$s of this type of SSMs are the Identity Matrices.

C. **Singular Value Decomposition based Traditional Space Vector Modulation**

Suppose the desired transfer function is
The peak values of the CMV for three types of switch states are calculated accordingly as below [29].

\[
v_{cm} = \frac{v_{oc} + v_{og} + v_{oc}}{3} \quad \text{for Type I Switch States},
\]

\[
v_{cm} = \frac{v_{oc}}{\sqrt{3}} \quad \text{for Type II Switch States},
\]

\[
v_{cm} = 0 \quad \text{for Type III Switch States},
\]

where \(v_{oc}\) is the amplitude of the input phase voltage. As can be seen, the Type III switch states have preference over the others, although they were not well explored. Since the CMV depends on the switch states of the converter, it is preferable to choose those states with low CMV magnitude and low voltage transitions whenever possible.

### A. Principle of replacement

Note that there exists an interesting relationship between the SSMs of the last two types switch states, as expressed in the following equations,

\[
\begin{align*}
S_{abc} &= S_{abc} + S_{bac} = S_{acb} + S_{cba}, \\
S_{cab} &= S_{cab} + S_{abc} = S_{bca} + S_{acb}, \\
S_{bca} &= S_{bca} + S_{abc} = S_{cab} + S_{acb}, \\
S_{abc} &= S_{abc} + S_{bac} = S_{cab} + S_{acb}, \\
S_{cba} &= S_{cba} + S_{abc} = S_{cab} + S_{acb}, \\
S_{cab} &= S_{cab} + S_{bac} = S_{acb} + S_{cba}.
\end{align*}
\]

Each Type III switch state is equivalent to two different switch state couples, each of which contains two Type II switch states. Once both switch states can be obtained, it is possible to replace them by their Type III equivalent, hence curtail that part of the CMV to zero.

To start with, one of the Type III switch states that rotate the input voltage space vector \(\vec{v}_i\) to the sector of the output voltage space vector \(\vec{v}_o\) is selected, as summarized in Table III. Here the sector division for the \(\vec{v}_o\) is the same as that for the \(\vec{v}_a\) rather than that for the input current space vectors. It

### III. COMMON-MODE VOLTAGE REDUCED SPACE VECTOR MODULATION

For motor drive systems it is important to reduce the CMV generated by power converters. Since it is common to connect the motor frame to the ground, the leakage current due to the CMV flows through the parasitic capacitor coupling to the rotor. High leakage currents can lead to early failures of winding insulation and motor bearings. In that the sum of the output currents approaches zero, the CMV then becomes,

\[
\begin{bmatrix}
\cos \alpha & -\sin \alpha \\
\sin \alpha & \cos \alpha
\end{bmatrix} \begin{bmatrix} g_a & 0 & g_a \end{bmatrix} = \begin{bmatrix}
\cos \theta & -\sin \theta \\
\sin \theta & \cos \theta
\end{bmatrix} \begin{bmatrix} v_a & 0 & v_a \end{bmatrix},
\]

where \(\alpha\) and \(\beta\) are the angles of the reference vectors with respect to the beginning of their corresponding sectors, \(\alpha_0 = 0\), the q-axis averaged gain \(g_a\) equals to zero. Hence, the output voltage reference \(\vec{v}_o\) is always located in the d-axis of the matrix \(\vec{v}_o\), while the input current reference \(i_f\) placed in the d-axis of the matrix \(\vec{V}\), as shown in Fig. 3. Denoting both equivalent direction reference space vectors in Fig. 2, the continuously rotating \(\vec{U}\) and \(\vec{V}\) can be approximated by two adjacent rotation vectors respectively. Therefore, four Type II switch states and one Type I switch state are selected in accordance with the locations of the reference vectors. For example, when both the input and output reference quantities lie in the Sector I, since the vectors directing to the points (1), (2) and (3) are used, taking account of the mutual match between the vectors shown in Fig. 2 and the SSMs listed in Table II, the switch states \(S_{abc}, S_{bac}, S_{cab}\) and \(S_{sac}\) are selected. Their duty cycles and the dutycycle for the zero vectors are calculated correspondingly to synthesize the local-averaged matrices \(\vec{U}, \vec{V}\) and \(\vec{D}\),

\[
\begin{align*}
\vec{U} &= \begin{bmatrix}
\cos \alpha & \sin \alpha \\
-\sin \alpha & \cos \alpha
\end{bmatrix}, & \vec{V} &= \begin{bmatrix}
\cos \theta & \sin \theta \\
-\sin \theta & \cos \theta
\end{bmatrix}, & \vec{D} &= \begin{bmatrix}
g_a & 0 & g_a \\
0 & g_a & 0
\end{bmatrix},
\end{align*}
\]

where the \(\alpha_v\) and \(\theta_v\) are the angles of the reference vectors with respect to the beginning of their corresponding sectors, the modulation index \(m\) is used to adjust the amplitude of the output voltages. The only limitation for \(m\) is to maintain the duty cycles in Eq. (5) as nonnegative.

The switching sequence among different switch states are also arranged, with one zero switch state employed, as shown in Fig. 4 [28]. When the sum of two sector numbers is even, a “u” shape switching pattern is utilized. Otherwise, if the sum of two sector numbers is odd, an “n” shape pattern is used.
means that the range from 0 to 60° in the complex plane is the first sector for $\vec{v}_i$.

Once the Type III switch state is chosen, the next step is to find its Type II equivalents. As can be seen from Equ. (8), one switch state within each couple is always contained in the four that are selected by the traditional SVM. As discussed in Section II-C four switch states with any two of which sharing one direction vector in at least one hexagon can synthesize two vectors in the input hexagon and two vectors in the output hexagon. According to the directions of these coupled switch states, two more supplementary switch states can be picked up to make up two direction vectors synchronously in both hexagons. Then these two vectors can be used to synthesize the rotational $\vec{U}$ and $\vec{V}$, together with other active vectors if needed. After the duty cycles for all required switch states are calculated, the corresponding Type II switch states can be combined as their equivalent Type III switch state.

Within both switch state couples of the Type III switch state, only one is used in this work to reduce the switching number. The one whose combined effective vectors are close to both $\vec{U}$ and $\vec{V}$ is selected for extended replacement.

**B. Example**

For convenience, we elucidate the proposed algorithm with the case that the input voltage space vector and the reference vectors $\vec{U}$ and $\vec{V}$ are all located in Sector I as an example. Four switch states $S_{abc}, S_{dab}, S_{ace}$ and $S_{bce}$ have been chosen by the conventional SVM as discussed in Section II-C.

Since the input and the output voltage vectors are located at the same sector, the Type III switch state $S_{abc}$ is selected. Then two switch state couples $S_{abc} = S_{ace} + S_{bce}$ and $S_{abc} = S_{dab} + S_{bce}$ are possible for substitution. For the former couple, the Type II switch state $S_{ace}$ points to the vector (1) in the input hexagon and the vector $\odot$ in the output hexagon while the $S_{bce}$ points to (3) and $\odot$. The vectors pointing to (1), (3) and $\odot$, $\odot$ are selected for synthesizing. Since only the $S_{ace}$ is within the four chosen switch states, three more switch states $S_{bce}$, $S_{ace}$ and $S_{bce}$ are needed to synthesize the blue vectors shown in Fig. 5. The last two switch states point to (3)$\odot$ and (1)$\odot$. On the contrary, the latter couple needs two more switch states $S_{bac}$ and $S_{bce}$ which direct to (1)$\odot$ and (2)$\odot$ respectively to synthesize the blue vectors shown in Fig. 6. This is because that the switch states $S_{bce}$ and $S_{bac}$ pointing to (1)$\odot$ and (2)$\odot$ have already been within the four chosen Type II switch states. For the former couple, the resultant direction vector at the input hexagon is in Sector II which is different from that of $\vec{V}$, while for latter couple the resultant vectors at both hexagons are in the same sectors where the reference $\vec{U}$ and $\vec{V}$ locate. Thus, $S_{abc} = S_{ace} + S_{bce}$ is chosen.

It should be noted that duty cycles for the switch states in Equ. (8) are equal. The switch states to make up the blue vector shown in Fig. 6, i.e. $S_{abc}, S_{dab}, S_{ace}, S_{bce}$ share the same

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**Fig. 5. Synthesis scheme for Combination $S_{abc} = S_{ace} + S_{bce}$.
Fig. 6. Synthesis scheme for Combination $S_{abc} = S_{dab} + S_{bce}$.
Fig. 7. Vector Synthesis when $\vec{U}$ is in the first half sector.**
TABLE IV
SWITCHING PATTERN IF \( U \) IS IN THE 1ST HALF SECTOR

<table>
<thead>
<tr>
<th>Switch</th>
<th>( S_{abc} )</th>
<th>( S_{acb} )</th>
<th>( S_{bac} )</th>
<th>( S_{ba} )</th>
<th>( S_{ab} )</th>
<th>( S_{a} )</th>
<th>( S_{b} )</th>
<th>( S_{c} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Duty-cycle</td>
<td>( d_{0}/4 )</td>
<td>( d_{0}/4 )</td>
<td>( d_{0}d_{y} )</td>
<td>( d_{0}d_{y} + d_{0}d_{z} )</td>
<td>( d_{0}/4 )</td>
<td>( d_{0}/4 )</td>
<td>( d_{0}/4 )</td>
<td>( d_{0}/4 )</td>
</tr>
</tbody>
</table>

TABLE V
SWITCHING PATTERN IF \( U \) IS IN THE 2ST HALF SECTOR

<table>
<thead>
<tr>
<th>Switch</th>
<th>( S_{abc} )</th>
<th>( S_{acb} )</th>
<th>( S_{bac} )</th>
<th>( S_{ba} )</th>
<th>( S_{ab} )</th>
<th>( S_{a} )</th>
<th>( S_{b} )</th>
<th>( S_{c} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Duty-cycle</td>
<td>( (d_{0} - d_{ac})d_{a} )</td>
<td>( d_{a}d_{x} )</td>
<td>( d_{0}/4 )</td>
<td>( d_{0}/4 )</td>
<td>( d_{0}/4 )</td>
<td>( d_{0}/4 )</td>
<td>( d_{0}/4 )</td>
<td>( d_{0}/4 )</td>
</tr>
</tbody>
</table>

Fig. 8. Vector Synthesis when \( U \) is in the last half sector.

Since all of them share the same \( \sigma_{c} = 0 \), the same modulation index \( m \) can be multiplied to the transfer function matrices of all the switch states used to regulate the amplitude of the output voltages. In the end, the Type II switch states \( S_{ab} \) and \( S_{bc} \) with same duty-cycle can be combined as their equivalent Type III switch state \( S_{abc} \). Therefore, the duty cycles and the switching sequence pattern for the used switch states can be found in Tab. IV.

Similarly, if \( U \) is in the second half of its sector, then the maximum duty-cycle for \( S_{abc} \) is \( d_{ac}d_{a} \), as shown in Fig. 8. The switch state \( S_{abc} \) disappears since its effect is replaced by the switch states \( S_{ab} \) and \( S_{bc} \). The rest of vector pointing to both (2) and (4) is performed by the switch state \( S_{abc} \) with duty cycle \( (d_{ac}d_{a}) \). Two pairs of Type II switch states with reverse directions are selected to replace the zero vector for switching sequence arrangement, which is slightly different from the case when \( U \) is in the first half sector. The duty cycles and the switching sequence pattern for all switch states can referred to Table V.

IV. EXPERIMENT RESULTS

Experiments are carried out to verify the feasibility of the proposed algorithm. The switch array of the MC consists of twelve bi-directional insulated-gate bipolar transistor (IGBT) switch SK60GM123 from SEMIKRON. The control platform is composed by a development starter kit 6713 (DSK) from Spectrum Digital and a field programmable gate array (FPGA) daughter board. The SVM algorithms are implemented using the Texas Instruments (TI) digital signal processor (DSP) TMS320C6713 on the DSK. The FPGA A3P400 from Actel is used to implement the four-step current commutation [30] and generate the gate drive signals...
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for the IGBT. The complete prototype system is shown in Fig. 9. Since we focus on the CMV suppression in this work, the modulation index is set fixed to avoid the interference of constant power loads which will be introduced by the fast closed-loop control strategies or feed-forward compensation by modulations [31]. For simplicity, the input current modulation strategy is set to give unit input power factor. The system parameters used are listed below:

1) three-phase supply with its phase voltage RMS of 110V at 50Hz fundamental frequency; 2) input filter inductor of 1mH, input filter capacitor of 9µF; 3) output frequency of 30Hz; 4) sampling frequency of 10kHz; 5) three-phase RL load in Y-type connection with $R_o = 50\, \Omega$ and $L_o = 15\, \text{mH}$.

Fig. 10 shows the waveforms for the converters with index $m = 0.7$. Both methods work well to maintain the source and output currents sinusoidal. The peak value of CMV is reduced by about 42% from 156V in Fig. 11(a) to 90V in Fig. 11(b). Note that ringing effect can be observed in the CMV waveforms due to the inductor at the loads. This effect extends the peak-to-peak value of the CMV. But even taking this effect into account, our proposed method has smaller CMV peak than the conventional SVM. As can be observed from the detailed CMV waveforms shown in Fig. 11, parts of the instantaneous CMV in every switching period are reduced to zero when our proposal is employed, which can not be seen in the conventional SVM. The RMS of the CMV have been also decreased by 20.3% from 93.7V for the tranditional SVM to 74.4V for the proposed SVM method.

Similarly, experiments are carried out under the condition of modulation index $m = 0.5$, as shown in Fig. 12. As can be seen, both methods can generate sinusoidal output currents, at the same time maintain the input current in good quality. The experiment results also validate that the proposed method are feasible to work in both high and low VTR applicatons. The CMV waveforms and their zoomed views are also given in Fig. 13. Similar peak value reduction, i.e. 42.3% can be achieved. Further, more reduction on the RMS of the CMV, up to 38.4% from 115.2V for the conventional SVM to 70.9V for the proposed method, can be obtained. Once again, the type III switch states that are with zero CMV can be observed in every switch sequence of the proposed method from the zoomed view shown in Fig. 13(b).
V. CONCLUSIONS

An SVM algorithm based on SVD technique to reduce the high-frequency CMV at the output of matrix converters has been proposed. In comparison of the traditional SVM, the switch states that connect each output line to a different input line are included in the switching sequence by combining two of their equivalent switch states. The CMVs are suppressed to zero during the time intervals for these switch states that are not used in the traditional SVM methods. As much as 42% reduction on the peak value and 20.3% reduction on the RMS of the CMV can be achieved. Therefore, the proposed method outperforms the traditional SVM in generating lower CMV.

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system control.