A Digital Self-Sustained Phase Shift Modulation Control Strategy for Full-Bridge LLC Resonant Converter

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Abstract

A digital self-sustained phase shift modulation (DSSPSM) strategy that allows for good soft switching and dynamic response performance in the context of step variations is presented in this paper. The working principle, soft switching characteristics, and voltage gain formulae of the LLC converter with DSSPSM have been provided separately. Furthermore, the method for realizing DSSPSM is proposed. Specifically, some key components of the DSSPSM are carefully investigated, including parameter variation analysis, start-up process, and zero-crossing capture of the resonant current. The simulation and experiment results verify the feasibility of the proposed control method; it is observed that the zero voltage switching of the switches and zero current switching of the rectifier diodes can be easily realized in context of step load variations.

Key words: LLC resonant converter, Soft switching, Dynamic response, Step load variations, Traveling-wave tube microwave transmitter, Phase shift modulation

I. INTRODUCTION

The traveling-wave tube (TWT) microwave transmitter has a wide bandwidth and a high gain, and it can be used for various applications, including communication, radar, electronic countermeasure, and space applications. The power converter is one of the key modules of microwave transmitter, which is used to power the TWT. With the development of modern microwave systems, some parameter criterions of TWT power converter are gradually increasing, including efficiency, power density, and dynamic response [1]-[3]. The resonant converter topologies are usually adopted to meet the high efficiency requirement of the TWT power converter, such as the parallel resonant converter, LLC resonant converter, and full-bridge phase-shift converter [4]-[5]. Moreover, LLC resonant converter has been attracting more and more attention for its inherent merits, including high efficiency, high power density, soft switching, and low EMI [6]-[10]. Therefore, the LLC converter is a preferred candidate for a microwave transmitter.

The TWT is a special load for the power converter. The TWT load is prone to sudden and repeated change with pulse modulation of pulsed microwave transmitter. Considering these step load variations, the power converter should be of good dynamic response and soft switching characteristics. At present, the power converter has not been studied in context of such step load variations widely, especially with respect to transient soft switching. To overcome these drawbacks, the converter topology should be improved, and the novel applicable control strategy should be developed [11]-[14].

The self-sustained phase shift modulation (SSPSM) has been proposed for resonant converters in [15] and [16]. This control scheme is inspired by the timing signal from the resonant current. In this manner, the control system is insensitive to the parameter uncertainties, and the gate pulses of the switches can be changed adaptively according to the operating condition. As opposed to the conventional frequency modulation (FM) control, SSPSM has much smaller frequency variation range [15], which makes it easy to optimize the magnetic components and realize miniaturization. As opposed to the conventional phase shift modulation (PSM) control, SSPSM can improve the soft switching in a wide operation range, which can achieve higher efficiency [15].

There has been considerable research on the SSPSM
The working principle and design method of full-bridge LCC converter under SSPSM have been proposed in [15]-[17]. The sliding-mode control of full-bridge LCC converter under SSPSM has been introduced in [18]. These references mainly concentrate on the basic working principles of full-bridge LCC converter under SSPSM, in which the characteristics of SSPSM associated with the parameter variations have not been widely analyzed. Besides, in these references, the SSPSM is realized by analog circuits, which are quite complicated, and some control functions are difficult to implement. For example, the loop for compensating the sawtooth wave adaptively is difficult to achieve. Consequently, the digital self-sustained phase shift modulation (DSSPSM) used for other novel converter topologies in context of parameter variations need to be investigated further.

The major contribution of this paper is the design and development of a novel DSSPSM control strategy. Some new technical factors of DSSPSM, which are used for the LLC converter in context of the step load variations have been proposed. First, the working principle of LLC converter with DSSPSM is discussed, which provides new insights into the improvement of soft switching and dynamic response characteristics of LLC converters. Second, the parameter design method of DSSPSM is presented, which is used to implement the soft switching. Third, the concrete realization method of DSSPSM is elaborated, especially in the applications associated with parameter variations. Finally, the transient soft switching of resonant converter is analyzed and evaluated.

The rest of this paper is organized as follows. We discuss the full bridge LLC resonant converter under DSSPSM in Section II. After that, we present the hardware and software realization of the DSSPSM in Section III. Then, we elaborate key parts of the DSSPSM design in Section IV. Simulation and experimental results are given in Section V. Finally, some concluding remarks are provided in Section VI.

II. FULL BRIDGE LLC RESONANT CONVERTER UNDER DSSPSM

A. Circuit Analysis

Fig. 1 shows the schematic of the proposed full-bridge LLC converter with voltage multiplier rectifier under DSSPSM. Switches pairs $Q_1$ and $Q_2$ as well as $Q_3$ and $Q_4$ form the full-bridge inverter. The resonant inductor $L_r$, transformer magnetic inductor $L_m$, and resonant capacitor $C_r$ form the LLC resonant tank. The diodes $D_1$, $D_0$, and capacitors $C_3$ and $C_1$ form the symmetrical multiplier rectifier. The DSSPSM and proportional plus integral (PI) control are adopted to implement the feedback control.
C. Soft-Switching Analysis

1) ZVS Analysis of the Switches

In order to realize ZVS of the switches, according to Fig. 2, the polarity of the resonant current \(i_{tr}\) should be kept in the dead time \(T_d\) between \(Q_1\) & \(Q_2\) or \(Q_3\) & \(Q_4\), and the limited condition is given by

\[
T_d < t_b - t_a
\]  

(1)

The function can be further expressed as

\[
T_d < \left(1 - \frac{v_a}{V_p}\right) \frac{1}{2f_s}
\]  

(2)

where, \(f_s\) is the switching frequency, \(V_p\) is the amplitude of the sawtooth wave \(v_a\).

Function (2) can be realized by selecting suitable parameters. In this situation, the resonant current \(i_{tr}\) lags behind the inverter output voltage \(v_{ab}\) and the zero crossing points of the resonant current are within the inverter output voltage pulse \(v_{ab}\). When one switch is turned on, the resonant current flows through the antiparallel body diode of this switch, and then the drain-source voltage of the switch is clamped to zero. In this case, the ZVS can be implemented.

2) ZCS Analysis of the Rectifier Diodes

Under DSSPSM, if \(\gamma_a - \gamma_b > 0\), the period that \(v_{ab} = 0\) is certain to exit in one switch cycle. In Fig. 2, \(T_s\) represents the period that \(v_{ab} = 0\). At the beginning of \(v_{ab} = 0\) (such as the moment \(t_0\) in Fig. 2), if \(i_{tr} = i_{lam}\), the converter has entered into the three component resonance. If \(i_{tr} > i_{lam}\), the load power is supplied by the LC \((L_r\) and \(C_r)\) resonant tank, the resonant current \(i_{tr}\) will decrease fast, and soon \(i_{tr} = i_{lam}\). \(T_i\) represents this decreasing period, and if \(T_i > T_s\), the converter will enter into the three-component resonance.

In order to realize ZCS of the rectifier diodes, the three component resonance should always exit in one switch cycle, and the limited condition is given by

\[
T_i < t_b - t_a
\]  

(3)

The function can be further expressed as

\[
T_i < \left(1 - \frac{v_a}{V_p}\right) \frac{1}{2f_s}
\]  

(4)

Function (4) can be realized by selecting suitable parameters. In this situation, all rectifier diodes will be switched off with zero current reducing the reverse recovery losses of diodes which contributes to increased efficiency.

D. Modeling Analysis

In order to guide the circuit analysis and parameter design, based on First Harmonic Approximation (FHA) method [19][20], the LLC converter model under DSSPSM is built.

The fundamental component \(v_{ab1}\) of the inverter output voltage \(v_{ab}\) can be expressed as

\[
v_{ab1} = -\frac{\pi}{4} V_m \cos\left(\frac{\gamma_a - \gamma_b}{2}\right) \sin\left(\omega t - \frac{\gamma_a}{2}\right)
\]  

(5)
Effective value $V_{ab1}$ of $v_{ab1}$ is described as

$$V_{ab1} = \frac{2\sqrt{2}}{\pi} V \sin\left(\frac{\gamma_s - \gamma_h}{2}\right)$$

(6)

The symmetrical multiplier rectifier can be simplified as Fig. 4(a). The fundamental component $v_{s1}$ of the inverter voltage $v_c$ can be expressed as

$$v_{s1} = \frac{2V}{\pi} \sin(\omega t - \phi_h)$$

(7)

The RMS value ($V_{s1}$) of $v_{s1}$ is described as

$$V_{s1} = \sqrt{2}V_o / \pi$$

(8)

The fundamental component $i_{s1}$ of the inverter current $i_s$ can be expressed as

$$i_{s1} = \frac{\pi}{2} I_s \sin(\omega t - \phi_h)$$

(9)

The equivalent reflected impedance $R_{eq}$ of multiplier rectifier can be derived as

$$R_{eq} = \frac{V_{s1}}{i_{s1}} = \frac{4R}{\pi^2}$$

(10)

Through the above analysis, the equivalent circuit of the LLC converter can be shown as Fig. 4(b).

The equivalent reflected impedance $R_{ac}$ on the primary side of the transformer can be expressed as

$$R_{ac} = n^2 R_{eq}$$

(11)

The open loop transfer function of LLC resonant tank can be given as

$$G(j\omega) = \frac{j\omega L_m R_m}{j\omega L + \sqrt{1 + (j\omega C)^2}}$$

(12)

Considering (6), (8), and (12), the DC gain of the resonant tank can be obtained as

$$|G(j\omega)| = \left| \frac{nV_{s1}}{V_{ab1}} \right| = \frac{V_s}{V_{m}} 2 \cos\left[\frac{n}{\pi} (\gamma_s - \gamma_h)/2\right]$$

(13)

The DC gain of the LLC converter can be expressed as

$$M(k, F, Q) = \frac{V_{m}}{V_s} = \frac{2}{n} \cos\left[\frac{\gamma_s - \gamma_h}{2}\right] G(j\omega)$$

$$= \frac{2}{n} \cos\left[\frac{\gamma_s - \gamma_h}{2}\right]$$

$$= \sqrt{1 + \left(1 - 1/F^2\right)/k^2 + Q^2(F - 1/F)^2}$$

(14)

where, $F = f_s / f_c$, $k = L_m / L_c$, $Q = \sqrt{L_m / C}$, $f_s = 1 / 2\pi \sqrt{L_m / C}$.

According to (15), the voltage gain curves of full-bridge LLC converter with DSSPSM are plotted, as shown in Fig. 5. According to this figure, the voltage gain $M$ increases with respect to the increase of phase $\gamma_h$. By controlling the phase $\gamma_h$, $v_{ch}$ is controlled, and the converter can be regulated. In addition, as the frequency ratio $F$ decreases, the phase $\gamma_h$ varies little with the same gain change, and the gain range gets wide, as shown in Fig. 5(a). As the quality factor $Q$ increases, the voltage gain $M$ gets little, as shown in Fig. 5(b).

III. REALIZATION OF DSSPSM

A. Hardware Realization

Fig. 6 shows the hardware realization schematic of DSSPSM. Fig. 7 illustrates the main waveforms of DSSPSM based on DSP. DSP board by Texas Instruments, TMS320F2812, is primarily used to implement the control scheme. General timer of DSP event manager is set to the continuous incremental mode, and used to generate the sawtooth wave $v_{st}$. The comparison unit register CMPR1 and CMPR2 separately represent the modulation line $v_{st}$ and $v_{ch}$. The logic signal $v_{s1}$ and $v_{s2}$ are separately obtained by comparing $v_{st}$ with $v_{ca}$ and $v_{cb}$. The zero-crossing moment of resonant current can be captured by DSP, and then the signal $v_{s3}$ can be easily generated.

In Fig. 6, the logic signals $V_{s1}$, $V_{s2}$, and $V_{s3}$ can be converted to the drive signals LQ1–LQ4, through logic operation of NOT gate, NAND gate, and RS flip-flop. After that, the dead-time of LQ1-LQ4 is generated by the RCD circuit. Lastly, two drive chips Si8235 are used to drive the switches.
the captured period does not belong to predetermined scope, the timer counter will return to zero. If the captured period belongs to the predetermined scope, the zero-crossing moment of the resonant current can be captured, and the zero-crossing period can be calculated. If the captured period does not belong to the predetermined scope, the timer period register will be updated.

The program flowchart of timer underflow interrupt is relatively simple. The timer underflow interrupt is stimulated, when the timer counter becomes zero. The zero-crossing square wave \( V_{r3} \) is generated in this program, and then the ADC converter is stimulated by the timer underflow interrupt flag.

Fig. 8 shows the ADC interrupt program flowchart. The ADC interrupt is stimulated by ADC flag. After the sampled value is obtained, the feedback control signal can be calculated by the digital position PI control algorithm, and then the comparison register CMPR2 is updated by the feedback control value.

B. Software Realization

Fig. 8 shows the software realization flowcharts of DSSPSM. The software is mainly composed of the main program and the interrupt programs, and the interrupt programs consist of capture interrupt, timer-underflow interrupt, and analog-to-digital conversion (ADC) interrupt.

Fig. 8(a) shows the main program flowchart. The program initialization is carried out first, and then the main program will wait to respond to the interrupt flags.

Fig. 8(b) shows the capture interrupt program flowchart. The capture interrupt is stimulated at the zero-crossing moment of the resonant current. The zero-crossing moment can be captured, and the zero-crossing period can be calculated. If the captured period belongs to the predetermined scope, the timer counter will return to zero. If the captured period does not belong to the predetermined scope, the timer period register will be updated.

IV. KEY PARTS OF DSSPSM DESIGN

A. DSSPSM Design Regarding Parameter Variations

Parameter variations of the converter, such as step load variations, will bring some problems to the DSSPSM design. For instance, the sawtooth wave may have distortions. Fig. 9 shows the simulation results of the sawtooth wave when the load is changed repeatedly between 600 Ω and 1200 Ω every
2.5 ms. We can find that the amplitude of the sawtooth wave begins to change at the load change moment. This phenomenon may lead to some mistakes, and some measures should be taken.

As a result, the gate pulses of switches will be wrong. Besides, if the amplitude of the sawtooth wave is larger than the normal amplitude \( v_{ca} \) in the period \( T_c(k+1) \), this situation, the logic signal \( v_{c1} \) will not be obtained in a correct manner. As a result, the gate pulses of switches will be wrong.

As shown in Fig. 10(b), during the period \( T_d(k+1) \), the captured zero-crossing period \( T_d(k+1) \) is larger than the normal value \( T_d(k) \), and two sawtooth waves will appear in the period \( T_d(k+1) \). In this situation, the logic signal \( v_{c2} \) will be wrong. Besides, if the amplitude \( V_{p2} \) of the second sawtooth wave in the period \( T_d(k+1) \) is larger than the modulation line \( v_{cb} \), the logic signal \( v_{c2} \) can not be obtained in a correct manner.

In order to solve the two mistakes as shown in Fig. 10, some measures should be taken.

1) For the mistake as shown in Fig. 10(a), the parameter variations should be concerned when selecting the value of \( v_{ca} \) previously. The value of \( v_{ca} \) should be always less than the normal amplitude \( T_{pr} \) of sawtooth wave \( v_{st} \). Moreover, if the captured amplitude \( V_{p1} \) is less than \( v_{ca} \), the value of \( v_{ca} \) should be immediately updated as

\[
v_{ca} < V_{p1}
\]

2) For the mistake as shown in Fig. 10(b), if the captured zero-crossing period \( T_d(k+1) \) is larger than the normal value \( T_d(k) \), the value of \( T_{pr} \) should be immediately updated as

\[
T_{pr} > V_{p3}
\]

B. Start-up Process

There are several situations that warrant consideration in the start-up process.

1) The resonant current may not be regular and stable in the start-up process, and the DSSPSM may become unreliable.

2) The sudden power-on may impact the converter hardware, and for this, soft starting should be realized.

In order to solve these two problems, following measures should be taken.

1) In the start-up period, the traditional phase shift control is adopted at first. When the converter becomes stable, the DSSPSM control begins to work.

2) The control signal \( v_{cb} \) varies slowly from zero to the predetermined value, and the pulse width of the inverter output voltage \( v_{gb} \) becomes wider gradually. In this way, soft starting can be realized.

C. Zero-Crossing Capture

Zero-crossing capture is a vital part of the DSSPSM design. If the zero-crossing moment cannot be captured correctly, the DSSPSM may not work. Fig. 11 shows the zero-crossing detection circuit. The hall-effect current sensor TBC06DS3.3 is adopted to sample the resonant current, and the zero-crossing square-wave of the resonant current is obtained through the ultrafast comparator LT1720. However, the rising edge and falling edge of the square-wave may have some chattering. Therefore, the figuration function of this square-wave needs to be achieved through RC filter and NOT gate 74LS14. In this way, the zero-crossing signal can be obtained in a correct manner, and sent to the capture port of the DSP.

V. SIMULATION AND EXPERIMENTAL RESULTS

A. Simulation Results

In order to evaluate the performance of the proposed DSSPSM control strategy, different simulation results are
presented in this section. The simulations are performed in MATLAB/SIMULINK software.

The simulation and experiment are carried out on a 340 W LLC resonant converter with an input voltage of 270 V. The resonant frequency is set to 115 kHz with \( L_r \) as 64.6 \( \mu \)H and \( C_r \) as 30 nF. The magnetic inductor \( L_m \) is set to 200 \( \mu \)H, and, thus, \( L_r/L_m \) is 3.1. The main parameters of the designed converter are shown in Table 1.

<table>
<thead>
<tr>
<th>TABLE I</th>
<th>CONVERTER PARAMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage ((V_{in}))</td>
<td>270 V</td>
</tr>
<tr>
<td>Output voltage ((V_o))</td>
<td>450 V</td>
</tr>
<tr>
<td>Resonant inductor ((L_r))</td>
<td>64.6 ( \mu )H</td>
</tr>
<tr>
<td>Resonant capacitor ((C_r))</td>
<td>30 nF</td>
</tr>
<tr>
<td>Transformer magnetic inductor ((L_m))</td>
<td>200 ( \mu )H</td>
</tr>
<tr>
<td>Transformer turns ratio ((n))</td>
<td>1:1</td>
</tr>
<tr>
<td>Output capacitor ((C_o))</td>
<td>10 ( \mu )F</td>
</tr>
<tr>
<td>Constant angle ((\gamma))</td>
<td>170°</td>
</tr>
</tbody>
</table>

Fig. 12 shows the typical simulation waveforms of DSSPSM, including the resonant current \( i_{r3} \), sawtooth wave \( v_{ab} \), the drain-source voltage \( v_{so} \) of switch \( Q_2 \), the drain-source voltage \( v_{bo} \) of switch \( Q_4 \), and the inverter output voltage \( v_{ab} \). As can be seen, the simulation results are in accordance with the theoretical analysis.

![Fig. 12. Typical simulation waveforms of DSSPSM.](image)

Fig. 13 shows the simulation waveform of output voltage \( v_o \) with respect to step load variations. The load resistance is changed between 600 \( \Omega \) and 1200 \( \Omega \) every 2.5 ms. As can be seen, the output voltage \( v_o \) has a little ripple against the step load changes, and the converter stays stable in the entire process.

![Fig. 13. Simulation waveform of output voltage \( v_o \) with respect to step load variations.](image)

Fig. 14 shows the simulation waveforms of resonant current \( i_{r3} \) and inverter output voltage \( v_{ab} \) regarding step load variations. As can be seen, \( i_{r3} \) can keep lagging behind \( v_{ab} \) when the load resistance becomes larger or less. In this situation, when one switch is turned on, the resonant current flows through the antiparallel body diode, the drain-source voltage is clamped to zero, and then the ZVS can be realized.

![Fig. 14. Simulation waveforms of resonant current \( i_{r3} \) and inverter output voltage \( v_{ab} \) with respect to step load variations.](image)

B. Experimental Results

In order to investigate the performance of the proposed DSSPSM control strategy, a laboratory prototype has been built, as shown in Fig. 15. The parameters of the converter are listed in Table 1.

![Fig. 15. Laboratory prototype.](image)

1) Steady State Performance

Fig. 16 shows the experimental waveforms of resonant current \( i_{r3} \) and zero-crossing square signal \( v_{3s} \) at full load. As can be observed, there is no chattering in the rising edge and falling edge of \( v_{3s} \), and the zero-crossing moment can be correctly captured by DSP.

![Fig. 16. Experimental waveforms of resonant current \( i_{r3} \) and zero-crossing square signal \( v_{3s} \) at full load.](image)
Fig. 16 Experimental waveforms of resonant current $i_{Lr}$ and zero-crossing square wave $v_{r3}$.

Fig. 17 shows the experimental waveforms of resonant current $i_{Lr}$ and inverter output voltage $v_{ab}$ at full load, half load and light load (10% load). As can be seen, in different load conditions, $i_{Lr}$ can lag behind $v_{ab}$, and all switches can implement ZVS which reduces switching losses of switches.

Fig. 18 shows the experimental current waveforms of the rectifier diodes $D_5$ and $D_6$. (a) Full load, (b) Half load and (c) Light load (10% load).

2) Dynamic State Performance

Fig. 19 shows the transient waveforms of the reverse resonant current $-i_{Lr}$ and inverter output voltage $v_{ab}$ under conventional PSM in context of step load variations. As can be seen, the current $i_{Lr}$ cannot keep lagging behind the voltage $v_{ab}$, and sometimes the soft switching characteristic of the converter is not so good for the step load variations.

Fig. 20 shows the transient waveforms of the resonant current $i_{Lr}$, inverter output voltage $v_{ab}$ and the output voltage $v_o$ under DSSPSM regarding step load variations. Fig. 20(a) shows the waveforms when the load resistance increases. Fig. 20(b) shows the waveforms when the load resistance decreases. The load resistance is changed between 600 Ω and 1200 Ω, and the load changing transition time is less than 200 ns.

As can be seen, $i_{Lr}$ can keep lagging behind $v_{ab}$ for the step load variations, and ZVS can be always implemented. Also, the converter is of good dynamic performance, and the output voltage $v_o$ can be tightly regulated to 450 V. The response time is less than 150 μs, and the output voltage overshoot and undershoot are about 4 V, which is less than 1% of 450 V.
DSSPSM. In future work, we will be aiming for practical easy to test the steady converter. In addition, the simulated resistance load is used to Therefore, the proposed DSSPSM control strate switching characteristics in context of the step load variations.

under DSSPSM has good dynamic performance and soft rectifier under DSSPSM is introduced. The working principle, experimental results validate that the proposed LLC converter

3) Efficiency Analysis

Fig. 21 shows the efficiency curve according to the load. The figure indicates that the efficiencies under different load conditions are higher than 92%, and their variance is minimalistic. The soft switching of LLC converter with DSSPSM can be realized under different load conditions leading to an improved efficiency in a wide operation range.

![Efficiency Curve](image)

Fig. 21. Efficiency curve according to load.

VI. CONCLUSIONS

In this paper, a novel DSSPSM control strategy is proposed, and a full bridge LLC resonant converter with multiplier rectifier under DSSPSM is introduced. The working principle, soft-switching characteristic, and realization procedure of DSSPSM are separately analyzed. Simulation and experimental results validate that the proposed LLC converter under DSSPSM has good dynamic performance and soft switching characteristics in context of the step load variations. Therefore, the proposed DSSPSM control strategy is valuable for improving the efficiency and power density of the power converter. In addition, the simulated resistance load is used to represent a TWT in the simulation and experiment, which is easy to test the steady-state and dynamic-state performance of DSSPSM. In future work, we will be aiming for practical application of DSSPSM in the TWT microwave transmitter.

REFERENCES

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