Seamless Transfer of Single-Phase Utility Interactive Inverters with a Synchronized Output Regulation Strategy

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Abstract

This study presents a synchronized output regulation (SOR) strategy for controlling inverters operating in grid-connected and stand-alone modes. As a concept of networked dynamic systems, SOR involves nodes with outputs that are synchronized but display a desirable wave shape. Under the SOR strategy, inverter and utility are regarded as two nodes that comprise the simplest network. These two nodes work independently under stand-alone mode. An intermediate synchronization mode is highlighted because it is a standard SOR problem in the transition from stand-alone mode to grid-connected mode. In grid-connected mode, the inverter operates in a relatively independent way, with only the reference voltage changing for a general synchronization, in which the current between the inverter node and the utility node satisfies the required power injection. Such a relatively independent design leads to seamless transfer between operation modes. The closed loop system is analyzed in the state space on the basis of output regulation theory, which improves the robustness of the design. Simulations and experiments are performed to verify the proposed control strategy.

Key words: Microgrid, Seamless transfer, Single-phase inverter, Synchronized output regulation

I. INTRODUCTION

Concerns for the environment and the scarcity of fossil fuel reserves have brought increasing attention to renewable energy sources. Distributed generation (DG), referring to generation plants connected to a distribution system, is a method of integrating renewable sources and distribution systems; this method meets the need to produce energy that matches the demand and reduces losses during energy delivery [1]. DG units as renewable energy sources are often implemented using an inverter-based interface [2], which is connected to the grid to transfer energy in a grid-connected (GC) mode and supplies the local load demand when faults occur in a stand-alone (SA) mode. The control method for inverters should be changed according to the different working modes. A fast and smooth transition between modes, which has emerged as an important issue in recent years, helps prevent sudden voltage changes across critical local load or any sudden current change to the grid [3].

Under GC mode, inverters control the current to provide the grid with a current that matches the required active and reactive powers. Generally, the current control for three-phase inverters connected to a balanced grid is not difficult; an early survey in this field was published in [5]. In recent years, model predictive control for current control of three-phase inverters [6]-[11] has received increasing attention. Current control typically involves a proportional-resonant (PR) controller [12], [13] or a proportional-integral controller after a dq transformation with a virtual quadrature component [14] for a single-phase system. In SA mode, inverters control voltage to energize the load. This problem is inherent in conventional DC-AC inverter control, and it emerges in the control of UPS and driving AC motors. Generally, an outer voltage control loop provides the current command, for which an inner current control loop is formed with a fast response [15]. The harmonics are suppressed by the internal model control and repetitive
Another mode occurring in the transition from SA to GC is the synchronization mode, in which the inverter synchronizes the voltage of the point of common coupling (PCC) with the grid voltage. This synchronization is necessary for the connection to the utility and is similar to SA mode. When the grid is under abnormal conditions, the inverter switches from GC mode to SA mode within a certain amount of time. Islanding detection is critical to determining the proper mode for an inverter [18], [19].

Seamless transfer is desirable in the transition between different working modes. A seamless transfer algorithm can switch inverter operations from voltage control mode to current control mode, and vice versa, with minimum interruption to the local load and grid [20]; in the cited work, the transfer steps between GC and SA modes are presented, but controller designs are not issued. During the transition from GA to SA mode, grid disconnection occurs at the instant of zero current and may last for half a line frequency cycle. An intentional voltage control method was proposed in [21] to hasten this disconnection process, in which case the grid current reaches zero several milliseconds after the detection of a grid fault. A method for changing the reference voltage was proposed for the seamless transfer of a single-phase inverter [22] to ensure controller output invariance during mode transfer. An indirect current control method was presented in [23] and [24] for single-phase and three-phase inverters, respectively. The control strategy proposed in [25] reduces the over-voltage stress of renewable energy and critical load under grid fault. The proposed controllers are composed of an outer current control loop and an inner voltage control loop. The outer current control loop stops in SA mode and provides the voltage reference in GC mode; in such a case, the inverter always works in voltage control mode to ensure a seamless transfer. However, a direct analysis of stability and performance, as well as a systematic synthesis method for controllers, remains lacking because of factors such as the nonlinear calculations involved. These nonlinear factors were recently relaxed [26], and another controller design was issued. In [27], an improved indirect current control method was presented for three-phase inverters [27], and an inner capacitance current loop was introduced to widen the bandwidth of the voltage control loop; this work also conducted a comprehensive analysis of steady and transient states in the frequency domain. A PLL-based seamless transfer method was presented for three-phase inverters [28]. PLL was used for the synchronization mode and for holding the initial angle invariant at the beginning of the SA mode. A damping resistor was added in the capacitance branch of the LCL filter to enhance stability. Recently, uniform controllers for both GC and SA modes based on robust µ-synthesis and model predictive control were presented in [29] and [30], but these works did not address mode transfer.

A brief version of the current paper was presented at IEEE CDC 2015 [36]. For this work, we have made numerous improvements, including the following: a detailed design concept of a single-phase PLL is presented, the effects of the internal model controller on the inner loop are illustrated, and the simulation results are presented on the MATLAB/Simulink platform, along with the results of a comparative experiment.

In this work, we present a design method for the seamless transfer of single-phase inverters from the viewpoint of synchronized output regulation (SOR), which is aimed at not only synchronizing the outputs of a network of agents but also manifesting the target dynamics [31]. A whole single-phase plant can be treated as a simple network of two nodes: the inverter and the utility. In SA mode, the inverter operates on its own and outputs a sinusoid voltage for the load. In GC mode, the inverter operates in the SOR case and outputs a voltage for the load, which is not only sinusoid but also synchronized with the utility in the sense that the grid current converges to a predefined value.

The idea behind SOR is to adjust the output reference of the inverter (node) according to synchronization errors (such as current tracking errors) instead of directly changing the inverter controller. The same idea was adopted in [22] and [24], but the SOR-based controller design offers three important advantages: 1) The model-based design provides a rigorous analysis of stability and tracking performance. The internal model principle for output regulation ensures high design robustness without requiring the exact knowledge of grid inductance parameters, are necessary in decoupled current control in previous studies; 2) The inverter is relatively independent. This independence motivates stopping the PLL in SA mode, which avoids the tracking phase of faulty grids; 3) The design method is scalable and is thus easily extended to a network with multiple inverters, such as microgrids. Moreover, the proposed controller is simple, involving only two feedback scalar gains, although a complex controller is permitted to improve controller performance in cases involving numerous parameters.

The remainder of this paper is organized as follows. The system description is presented in Section II, along with the network perspective of the inverter plant and models of three working modes. The design seamless transfer controller based on SOR is described in Section III. Simulation results from the MATLAB/Simulink platform are illustrated in Section IV, followed by a scaled-down experiment in Section V. Conclusions are discussed in Section VI.

II. SYSTEM DESCRIPTIONS

The circuit topology of a single-phase utility connected inverter is shown in Fig. 1. A single-phase full-bridge voltage
source inverter (VSI) driven by a DC source, through an LC filter, connects to a load. It also connects to the grid via an extra inductance for harmonic suppression. A switch (SW) is located between the inductance and the grid. The inverter transmits power from the DC source into the utility power when the SW is activated in GC mode. When the SW is deactivated, the inverter supplies the power of the DC source for critical loads in SA mode.

A. Perspective for Two Nodes

The plant to be studied can be treated as a simple network system that consists of two nodes: the grid and the VSI with an LC filter. The two nodes are connected by an inductance and a switch, as shown in Fig. 2. The grid designated as node 0 has an output voltage, which is the grid voltage. The VSI designated as node 1 has an output voltage, which is the voltage of the filter capacitance. In any operating mode, the outputs of both nodes manifest the required sinusoids.

When two nodes are connected, their outputs should be synchronized in advance to avoid overcurrent at the connecting moment. This SOR problem was studied in [31] and [32]; specifically, it requires the outputs of all nodes to be regulated and synchronized to track a given waveform (sinusoids in this case) and thereby achieve a “cooperative output regulation.” One solution to the SOR problem is to track the reference signal with an output regulation method and to synchronize the reference signals through the feedback of synchronization errors. The control of the currents or voltages of VSI with an output regulation method was reported [16].

In the present work, the SOR strategy is applied to cope with the synchronization process before the connection of the VSI to the grid, as well as to control the GC mode and SA mode. This strategy provides the controller with a uniform structure for different operating modes to realize the seamless transfer of the plant shown in Fig. 1.

Another merit of using the SOR strategy is the treatment of the generation unit as a relatively independent node with a distributed controller; hence, the result is scalable and can be extended to DG and microgrids. This study considers three operating modes, which are described below.

B. Stand-Alone (SA) Mode

The switch is open in SA mode. Node 1 simply supplies power to the local load. In this study, VSI connects to the load through the LC filter, and the voltage is that of the filter capacitor. The dynamic model for node 1 is

$$\frac{di}{dt} = -\frac{R_1}{L_1}i_1 + \frac{1}{L_1}(u_i - u_c)$$

(1a)

$$\frac{du_i}{dt} = -\frac{1}{RC_f}u_i + \frac{1}{C_f}(i_1 - i_2)$$

(1b)

where \(i_1\) and \(i_2\) are the currents of inductances, \(u_c\) is the capacitor voltage, and \(u_i\) is the input of the LC filter that is treated as the equivalent output voltage of the VSI. In SA mode, \(i_2 = 0\). \(i_2\) remains in the dynamic model to maintain consistency for the following GC mode. The reference voltage \(u_c\) to be tracked by \(u_i\) is a sinusoid wave with the rated RMS \(V_c\) and angle frequency \(w_c\). In mathematics, \(u_c\) can be modeled by

$$\eta_c = \begin{bmatrix} 0 & w_c \\ -w_c & 0 \end{bmatrix} \eta_{cs}, \quad u_c = \sqrt{2}V_c \begin{bmatrix} 1 \\ 0 \end{bmatrix} \eta_{cs},$$

(2)

where \(\eta_{cs} \in \mathbb{R}^2\) and the initial condition is \(\eta_c(0) \in \Omega \triangleq \{x \in \mathbb{R}^2 : x'x = 1\}\). In output regulation theory, the above is an ecosystem that produces reference signals. The controller for SA mode aims to make \(e_s = u_c - u_i \rightarrow 0\).

C. Synchronization Mode

When SW is to be closed, the voltages on both sides of the switch should be synchronized in advance. In this mode, the dynamics of node 1 are the same as those in SA mode, but the goal is changed to make \(e_s = u_c - u_i \rightarrow 0\), where \(u_s\) denotes the grid voltage and can be modeled by

$$\begin{bmatrix} 0 & w_s \\ -w_s & 0 \end{bmatrix} \eta_{ss}, \quad u_s = \sqrt{2}U_s \begin{bmatrix} 1 \\ 0 \end{bmatrix} \eta_{ss}$$

(3)

where \(\eta_{ss} \in \mathbb{R}^2\) and voltage \(U_s\) denote the RMS value of the grid voltage.

To hold the controller invariant with respect to that in SA mode, along the solution of the SOR problem, \(e_s \rightarrow 0\) is realized by adjusting the dynamics of the exosystem \(\eta_s\) such that \(u_i \rightarrow u_s\).

Once synchronization is achieved, \(\|u_i - u_s\| \leq T_s\) for a predefined threshold value \(T_s\), SW is closed, and node 1
Fig. 3. Block diagram of the proposed controller, as well as the adopted PLL. The definitions of the selection signals Mode and Syn are detailed in Table I [36].

transitions to GC mode. Note that synchronization mode only occurs in the transition from SA mode to GC mode. As for the reverse transient phase that often occurs during grid faults, SW is required to deactivate as quickly as possible without additional considerations.

D. Grid-Connected (GC) Mode

In this mode, SW is closed, and node 1 provides the grid with the desired current and power for the local load. The phase angle of the grid voltage is set to zero, \( \bar{u}_g = U_g \angle \phi \), and the reference current \( i_r \) to be tracked by \( i_2 \) is given by \( \bar{i}_r = I_r \angle \phi \), where \( I_r \) represents the RMS value and \( \phi \) represents the phase angle between the voltage and the current. Similar to \( u_s \), \( i_r \) is modeled by

\[
\eta_i = \begin{bmatrix} 0 & w_s \\ -w_s & 0 \end{bmatrix} \eta_i, \quad \text{with} \quad \eta_i(0) = \begin{bmatrix} \cos \phi \\ \sin \phi \end{bmatrix}
\]

\[
i_r = \sqrt{2} I_r \begin{bmatrix} 1 & 0 \end{bmatrix} \eta_i
\]

where \( \eta_i \in \mathbb{R}^2 \) is the state. The requirement of the phase angle is reflected by initial conditions \( \eta_i(0) \) and \( \eta_u(0) \) in (3). Note that both \( \eta_i \) and \( \eta_u \) are used only for theoretical analysis and are not needed for controller implementation.

In this case, the dynamic model of node 1 is invariant with the following augmented dynamics of \( i_2 \):

\[
\frac{d i_2}{dt} = -\frac{R}{L_2} i_2 + \frac{1}{L_2} (u_r - u_s).
\]

The goal of the controller for GC mode is to achieve \( e_i = i_2 - i_r \to 0 \). Similarly, the controller is held invariant \( e_i \to 0 \) by adjusting the exosystem \( \eta_e \) indirectly.

III. CONTROLLER DESIGN

The controller structure is shown in Fig. 3, in which the controller can be divided into two parts, namely, the inner voltage control loop and the outer current control/synchronization control loop. “Mode” denotes the three operation modes of the study case (Table I). The outer loop is a simple integrated feedback, the gain \( k_e \) of which is to be determined. This loop works for the GC mode (Mode=3) and synchronization mode (Mode=2).

The outer loop works under the current control mode when Mode = 3. Reference voltage \( u_e \) is adjusted by the current tracking error \( e_i \). Reference voltage \( u_e \) is adjusted for tracking grid voltage \( u_g \) when Mode=2.

If Mode=1, then only the inner voltage control loop is operating. The zero selection signal Syn makes the output of the integrator invariant, as does \( \eta_u \), which is scaled by scalar \( V^* \) to ensure the rated load voltage; \( V^* \) denotes the peak value of the rated voltage. The zero Syn causes the PLL to shut down. The reference frequency \( w_0 \) is the nominal \( w_f \). The reference voltage, at the instant of transition from GC to SA mode, shows an invariant phase but rotates at a nominal speed. As a result, the transfer from GC mode to SA mode is smooth, and the deterioration of load voltage is minimized.

Our design solves the SOR problem by adjusting the reference voltage to allow the controller to adapt to different operating modes. This adjustment does not influence the design of the inner voltage control loop; hence, different feedback gains need not be designed for different modes.

<table>
<thead>
<tr>
<th>Mode</th>
<th>Stand-alone</th>
<th>Synchronization</th>
<th>Grid-connected</th>
</tr>
</thead>
<tbody>
<tr>
<td>Syn</td>
<td>0</td>
<td>1</td>
<td>3</td>
</tr>
<tr>
<td>SW</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

TABLE I
VALUES OF SELECTION SIGNALS AND THE SWITCH IN THE VARIOUS OPERATION MODES [36]
Moreover, the proposed controller shows a uniform structure for different operating modes. The controller is concise, as only two parameters $k_c$ and $k_i$ need to be designed (Fig. 3) for the outer loop controller and inner loop controller, respectively. The parameter $i$ is used to enhance the damping of the output loop, and it may be removed in the presence of $\frac{2}{R}$, as demonstrated in the following.

### A. PLL

In practice, the frequency of the utility is not fixed but fluctuates around the rated frequency. The PLL circuits or algorithm should thus obtain the utility frequency and phase angle necessary for synchronization and GC mode. We adopt a single-phase PLL that is based on a second-order generalized integrator (Fig. 4).

The PLL has outputs $\theta$ and $w_r$. For the former, $u_g(t) = \sqrt{2}U_g \cos \theta(t)$, from which the desired current in GC mode can be obtained by

$$i_s = \sqrt{2}I_s \cos (\theta(t) + \phi) = \sqrt{2}I_s \cos (\theta(t)) \cos \phi - \sin (\theta(t)) \sin \phi.$$  

(6)

The angle frequency $\omega_e$ used for the artificial exosystem of node 1 is used to build the internal model controller. A low pass filter is introduced to make $\omega_e$ vary slowly and thereby allow $\omega_e$ to be approximated as a constant scalar in the theoretical analysis.

In SA mode, zero signal Syn ceases PLL. Subsequently, node 1 works independently with $w_r = w_f$, which represents the rated line angle frequency.

### B. Internal Model Controller for Inner Loop

The inner loop controller, the structure of which is illustrated in Fig. 5, is based on the internal model principle.

Noting that $i_s$, which is treated as a disturbance with respect to node 1, comes from the same dynamic mode as that for the reference voltage $u_r$, the internal model to be embedded in the controller is the same as that in (2). The dynamic controller shows the form

$$\dot{z} = S(w_e)z + G\eta_e, \quad u_i = -k_i G^T z$$  

(7)

where $S(w_e) = \begin{bmatrix} 0 & w_e \\ -w_e & 0 \end{bmatrix}$. As any nonzero $G$ may be used for the controllability of pair $(S,G)$, $G$ can be selected arbitrarily. Positive scalar $k_i$ is a tuning parameter. The utility of the dual $G$ and $G^T$ design is to provide passivity to controller (7). With this controller, the closed loop system in SA mode is described as

$$\dot{x} = A x + k_i B G^T z, \quad \dot{z} = S(w_e)z + G(C x - Q \eta_e)$$  

(8)

where $x = [i_s, u_f]^T$ and

$$A = \begin{bmatrix} \frac{L_i}{C} & -\frac{1}{C} \\ \frac{1}{L_i} & \frac{1}{C R} \end{bmatrix}, \quad B = \begin{bmatrix} 1 \\ 0 \end{bmatrix}, \quad C = [0 \ 1], \quad Q = \begin{bmatrix} 2\sqrt{2} & 0 \end{bmatrix}$$

The following result is directly obtained from the output regulation literature [33].

**Theorem 1:** If feedback scalar $k_i$ is such that the following matrix

$$A_m = \begin{bmatrix} A & -k_i B G^T \\ C & S(w_e) \end{bmatrix}$$  

(9)

is Hurwitz, then the voltage tracking error $e_v$ exponentially converges to zero under controller (7).

Normally, the voltage of VSI comprises harmonic components. According to SOR theory, the harmonic components can be treated as disturbances. The disturbances can be rejected by designing $S(\omega_e)$ with corresponding internal models.

### C. Outer Loop Design

1) **Synchronization mode:** In synchronization mode, the dynamics of node 1 are the same as those in SA mode, except the dynamics of exosystem $\eta_e$ become

$$\dot{\eta}_e = S(w_e)\eta_e + L (u_r - u_e)$$  

(10)

where $L \in \mathbb{R}^2$ is a row vector to be determined. Evidently, the feedback term in the above system makes $u_r \rightarrow u_e$, which is guaranteed by the following result.

**Lemma 1:** Assume that $u_e = Q \eta_e$ for some row vector $Q \in \mathbb{R}^2$. If $L$ is such that $S(w_e) + LQ_e$ is Hurwitz, then $u_r - u_e$ exponentially converges to zero for any $Q_e$.

**Proof:** There are two scalars $b_1$ and $b_2$ such that
Then, $\eta_g = S(w_i)\eta_{g'}$, and $u_i = Q\eta_g$. Noting that (10) is an observer of system $\eta_g$, $u_i - u_{i_0} \to 0$, with $S(w_i) + LQ_n$ being Hurwitz.

The dynamics of $\eta_n$ in (10) are independent of the inner loop dynamics. The whole closed loop system in synchronization mode is a cascaded connection of two exponential systems; hence, the following result can be obtained.

Theorem 2: If $k_i$ and $L$ are such that $A_n$ and $S(w_i) + LQ_n$ are Hurwitz, then $u_i$ exponentially converges to zero under the controller consisting of (7) and (10).

The matrix $L$ is a feedback gain of an observer, on the basis of which the optimal design can be applied. In this work, the gain is given by

$$L = -XQ_n^T$$

where $X$ is the solution of the algebraic Riccati equation

$$XS(w_i) + S(w_i)^TY - XQ_n^TQ_nX + I = 0$$

The nominal model of exosystem $S(w_i)$ is used instead of the real-time $S(w_i)$. As explained previously, the solution above achieves the largest robustness with respect to the uncertainties of $S(w_i)$ [34].

2) $GC$ mode: In this mode, the dynamics of exosystem $\eta_n$ and the reference voltage $u_i$ become

$$\dot{\eta}_n = S(w_i)\eta_n + k_iL\epsilon, \quad u_i = Q\eta_n - \epsilon e_i.$$  \hspace{1cm} (13)

where $L$ is as same as that in (11), with scalar $k_i$ as the tuning parameter to be designed, and positive scalar $\epsilon$ can be treated as the $L_2$ branch’s virtual resistance. The current error feedback changes the exosystem dynamics $\eta_n$ until the reference voltage produced by the exosystem is such that $e_i = 0$. An extra damping term $\epsilon e_i$ is added to regulate the convergence rate of the current control differently from the reference voltage in (2), which, in practice, may be zero if a large $R_2$ exists.

In this case, the analysis of the closed loop system is more difficult than that of the other two modes because the dynamics of node 1 and reference voltage $\eta_n$ are coupled via the nonzero current $i_2$ and especially because our design is based on holding the inner loop invariant and not on redesigning a current controller. This is the essential idea of SOR: VSI is treated as a node with an inner structure that cannot be altered; one can only revise the commands or the reference voltage.

In this mode, the closed loop system shows the following form:

$$\begin{align*}
\dot{x}_i &= A_n x_i - k_iB_iG^T z_i, \\
\dot{z}_i &= S(w_i)z_i + G(C_n x_i - Q_i\eta_n) + G(i_2 - i_i) \\
i_2 &= \frac{1}{L_2}C_n x_i - \frac{R_2}{L_2}i_i - \frac{1}{L_2}u_i \\
\dot{\eta}_n &= S(w_i)\eta_n + k_iL(i_2 - i_i)
\end{align*}$$

We define $x_i = [x_i^T; z_i^T]$ and $w_i = [\eta_n^T; \eta_{g'}^T]$. The above system can be rewritten in the following compact form, which is standard in output regulation theory.

$$\begin{align*}
\dot{x}_i &= A_d x_i + B_d(-Q_i\eta_n) + P_i w_i, \\
w_i &= S(w_i) \\
\dot{\eta}_n &= S(w_i)\eta_n + k_iL(C_n x_i - Q_i w_i)
\end{align*}$$

where

$$A_d = \begin{bmatrix} A_n & -k_iB_iG^T & 0 \\
GC_n & S(w_i) & \epsilon G & B_d = G \\
1 & 0 & -\frac{R_2}{L_2}
\end{bmatrix}, \quad P_d = \begin{bmatrix} 0 & 0 \\
-\epsilon G\sqrt{2I}I_{[1,0]} & 0 \\
0 & -\frac{1}{L_2}\sqrt{2U_iI_{[1,0]}} & 0
\end{bmatrix}, \quad S_d = \begin{bmatrix} S(w_i) & 0 \\
0 & S(w_i)
\end{bmatrix}, \quad C_d = [0_{1,2}, 1], \quad Q_d = \left[\sqrt{2}I, 0_{1,2}\right]
$$

Theorem 3: If $k_i$ is such that $A_{m_2} = \begin{bmatrix} A_n & -B_iQ_i \\
k_iLC_n & S(w_i)
\end{bmatrix}$ is Hurwitz, then the current tracking error $e_i$ exponentially converges to zero under the controller consisting of (7) and (13).

D. Mode Transfer Sequence

The sequences of mode transfer under the proposed controller (Fig. 3) are illustrated in this subsection.

Transfer from grid-connected mode to stand-alone mode

1) Detect a fault on the grid.
2) Set the synchronization signal $\text{Syn}=0$.
3) Provide a switch-off signal to switch SW.
4) Set Mode=1 to switch the operating mode of controller to stand-alone mode.

This sequence shows the controller gains and controller commands are unchanged in the transfer from grid-connected to stand-alone mode. In previous studies, PLL will lock on the phase of the capacitor voltage, requiring an extra step to gradually change the voltage reference; however, this is
TABLE II

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
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<tbody>
<tr>
<td>$R_1$</td>
<td>0.5Ω</td>
</tr>
<tr>
<td>$L_1$</td>
<td>1mH</td>
</tr>
<tr>
<td>$R_2$</td>
<td>0.3Ω</td>
</tr>
<tr>
<td>$L_2$</td>
<td>2mH</td>
</tr>
<tr>
<td>$C_f$</td>
<td>10μF</td>
</tr>
<tr>
<td>$R$</td>
<td>10Ω</td>
</tr>
<tr>
<td>$V_p$</td>
<td>220V</td>
</tr>
</tbody>
</table>

unnecessary in this paper.

If Syn=0, neither the PLL nor the outer loop will work, as the former indicates the frame of the synchronization reference is rotating at nominal speed, $\omega_f$, while the latter indicates the voltage reference $\eta_v$ will maintain its phase at the time that Syn changed from 1 to 0.

The reverse transfer is complex as it should experience an intermediate synchronization mode.

Transfer from stand-alone to grid-connected mode

1) Detect the grid recovers.
2) Set Mode=2 and detect synchronization error $u_c - u_g$.
3) Set Syn=1 to start the PLL and the outer loop.
4) If $\|u_c - u_g\|$ is less than some predefined threshold values for three periods, then turn on switch SW.
5) Set Mode=3, and switch the operating mode of the controller to GC mode.

In this transfer process, the controller gains have yet to be altered. The changes occur on the controller commands when Syn changes to 1 and when Mode changes from 2 to 3. The switch of Syn causes neither the jump of the output angle $\theta$ of the PLL nor the jump of input $u_i$, as only integrators exist in the channel from the signal Syn to $\theta$ and $u_i$ without any proportional gains.

E. Parameter Design

The proposed method only requires two designed scalar parameters, $k_i$ and $k_o$. Their design is decoupled, as $k_o$ can be selected after $k_i$, which is independent of $k_o$. If $k_i$ and $k_o$ are zero, then $A_{in}$ and $A_{ou}$ are critically stable, and the solutions of $k_i$ and $k_o$ always make $A_{ou}$ Hurwitz, respectively. The root locus analysis method is preferred for the scalar feedback gain design.

The electrical parameters are given in Table II. We first design the inner loop gain $k_i$. Fig. 6 shows the root locus of $A_{in}$ with $G=[3,-1]^T$. The start point $k_i=0$ has two pair complex eigenvalues from $S(u_c)$ located at the imaginary axis. As $k_i$ increases, they first tend to move to the left and then converge to negative infinity and origin zero, respectively, after $k_i>62$. The other pair from $A_u$ tends to move to the right and crosses the imaginary axis after $k_i>1040$. In this study, we select $k_i=500$.

For the design of $k_o$, we select $\epsilon=1$ and $L=[-1.36,0.38]^T$ calculated by (11). If $k_i=500$, then the root locus of $A_{ou}$ is shown in Fig. 7 with the rightmost pair complex eigenvalues $-4700 \pm 8000j$ omitted; these eigenvalues are almost fixed as $k_o$ varies. Except for the origin zero, an extra zero is located at the right half real axis. The largest allowable value of $k_o$ is 22.9.

Fig. 6. Root locus of $A_{in}$ as $k_i$ varies.

Fig. 7. Part root locus of $A_{ou}$ as $k_o$ varies.

For the design of $k_o$, we select $\epsilon=1$ and $L=[-1.36,0.38]^T$ calculated by (11). If $k_i=500$, then the root locus of $A_{ou}$ is shown in Fig. 7 with the rightmost pair complex eigenvalues $-4700 \pm 8000j$ omitted; these eigenvalues are almost fixed as $k_o$ varies. Except for the origin zero, an extra zero is located at the right half real axis. The largest allowable value of $k_o$ is 22.9.

$\epsilon=2.5$ is selected for the simulation.

F. Robustness Analysis

From the theoretical point of view of control, the output regulation design based on the internal model principle offers robustness to the output tracking problem. The essence of robustness here is that the no-bias output tracking problem is converted into a stabilization problem for an augmented linear system. When $A_{ou}$ remains Hurwitz under a certain perturbation of the parameters, the output performance is unchanged. The real stability radius of $A_{ou}$, denoted as $r_{stab}$, is often used as the maximum size of perturbation under which the system maintains stability [4]. Here, it is calculated as $r_{stab}=2.44$ and $\frac{1}{r_{stab}}=41\%$. Hence, $A_{ou}$ remains stable for any electrical parameter perturbation with a size of 41% or less.
Fig. 8. Complete simulation process.

Fig. 9. Transition from stand-alone mode to grid-connected mode. Brt is the switch signal for the circuit break, and FauU is the switch signal for the utility fault.

IV. SIMULATION EXAMPLE

A simulation using the above parameters is performed in the MATLAB/Simulink environment to verify the developed controllers. In the simulation, the constant DC source is 400 V, the voltage of the single-phase utility grid is 220 V at 50 Hz, and the switching frequency of the inverter is 6 kHz. In GC mode, the inverter energizes the local load and transfers energy into the utility. The desired current injected to the utility is \(I = 15 \angle \phi\) with \(\phi = 10^* \pi / 180\). The local load has a resistance of 10Ω.

The simulation process is shown in Fig. 8. At the first phase, from 0 ms to 250 ms, the inverter operates in SA mode, outputting the rated voltage for the local load. At 250 ms, the inverter detects the utility voltage. After two periods, the utility is confirmed to be normal, and the inverter enters synchronization mode to close the circuit break at 287 ms. Once the synchronization error is less than a predefined threshold, the inverter switches to GC mode at 350 ms. In GC mode, the inverter injects the desired current to the utility. At 600 ms, the utility is broken. The inverter detects this unintentional islanding via phase-jump detection [35] and returns to SA mode.

Fig. 9 shows an enlargement of the first mode transition from SA mode to GC mode. This transition is intentional and can thus be scheduled to be sufficiently smooth. However, a distortion of the load voltage arises at the beginning of synchronization mode because of the required short synchronization process, with which the whole simulation can be finished in less than 1 s.

After two periods of synchronization, the inverter output is synchronized with the utility voltage, and the signal SW jumps to 1 to close the single-phase circuit break. Subsequently, the current \(I\) injected to the utility arises, and the inverter enters GC mode.

Fig. 10 is an enlargement of the mode transition from GC mode to SA mode. The utility fault occurs at 605 ms with current \(i_2 = 0\). After the fault, \(u_c\) increases to a certain extent because of the detecting time or the interval between fault occurrence and detection, during which the controller continues operating in GC mode while \(i_2 = 0\). As a result, the capacitance absorbs the energy to be delivered to the utility such that its voltage rises. From this period, the true voltage is not the measured utility voltage \(u_c\) but the value of the capacitor voltage \(u_c\). This characteristic is shown in Fig. 10, where \(u_c\) coincides with \(u_c\) until the single-phase circuit break deactivates. This coincidence is the main difficulty of islanding detection.

The controller detects the utility fault at 612 ms, after which the inverter switches to SA mode. Fig. 10 shows that the load voltage \(u_c\) maintains the sinusoid waveform, except for an increasing magnitude in the short islanding detection phase. This seamless feature is caused by the phase of the reference voltage in the proposed controller being invariant during switching time and the PLL not being used in SA mode.

V. EXPERIMENT

An experimental validation is designed to further verify the developed controller. Specifically, the experiment is aimed at verifying the seamless transition performance of the hardware.
between different modes, whether from SA mode to synchronization mode or from synchronization mode to GC mode and GC mode to SA mode. The experimental hardware is shown in Fig. 13. The circuit topology of the hardware differs slightly from the simulated hardware. A tunable isolation transformer is added between the grid interface inductor and the grid in Fig. 1. Here, the ratio of the transformer is set to 30:220 so that the inverter rated output voltage is AC 30 V. The voltage of the DC bus is 50 V. The parameters of the experimental hardware and control algorithm are also different from those of the simulation, which are listed in Tables III and IV. As a result of practical limitations, some parameters of the real experimental platform are not the same as those of the simulation. The simulation accurately imitates high voltages and powers and can illustrate more information, as in the last section. The experiment highlights the successful results in the real scaled platform.

We select a mechanical relay as the grid connection switch. The switching frequency of the inverter is 20 kHz. In SA mode, the switch is turned off, and the inverter converts DC 50 V to AC 30 V to provide energy for local loads. When the switch is turned on under GC mode, it supplies local load and transfers 90 W active power to the utility via the transformer. The signal circuit is composed of a basic board and a control board. The signal circuit processes the sample signal from the voltage and current sensors in the power circuit and sends them to the controller. The control board contains a DSP28335 with peripheral circuits for the chip. We maintain the quality of the high-frequency switching signal by using fiber optic transmission between the signal circuit and the driving circuit of the inverter.

Fig. 12 illustrates the synchronization process that occurs during the transition from SA mode to synchronization mode. After the synchronization command (falling edge of the purple waveform) is sent, the output voltage (green waveform) reaches the grid voltage (yellow waveform) within 80 ms. Once synchronization is achieved, the switch is deactivated, and the inverter operates in GC mode with a mode change command (the falling edge of the purple waveform in Fig. 13). The current injected into the utility (green waveform) reaches the reference in 100 ms. In Fig. 12, an apparent deviation exists between uc and ug after synchronization; such deviation is not a deviation between phases but is a result of poor grid quality.

Fig. 13 exhibits the transition from GC mode to SA mode during an open circuit fault. The current (green line) quickly drops to zero, but the inverter continues in GC mode immediately after the fault, as the latter has not been detected. This improper control mode causes the output voltage to rise. Once the fault is detected, the mode change command (rising edge of the purple waveform) is sent, the inverter transitions from GC mode to SA mode, and the waveform of the output voltage restoration is stable in 60 ms. In Fig. 14, a distortion occurs in the current because of the aforementioned poor quality of the utility in the lab.
A comparative experiment using the PR controller under the same conditions is also performed. Figs. 15 and 16 show the transitions from SA mode to synchronization mode and from synchronization mode to GC mode. At 100 ms, a sharp distortion occurs in Fig. 15 during the transition while a delay exists in Fig. 16; the same processes in Figs. 12 and 13 are smooth. The rough transitions cause interruptions to the local load and the grid. As the method cannot achieve asymptotic tracking of the reference, errors persist between the grid and output voltages.

VI. CONCLUSION

This paper presents an SOR strategy for the seamless transfer of inverter control. The strategy treats the inverter as a relatively independent node in the sense that the operation mode changes influence the reference voltage but does not change the inverter controller, which is always controlling the voltage. This condition offers a smooth transition between modes. The analysis for the closed loop system in the different modes is built in the state space model. This work validates the controller through simulations and experiments. Our future studies will focus on the extension of the proposed strategy to multiple parallel inverters.

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