A Hierarchical Model Predictive Voltage Control for NPC/H-Bridge Converters with Reduced Computational Burden

Zheng Gong*, Peng Dai†, Xiaojie Wu*, Fujin Deng**, Dong Liu** and Zhe Chen**

†*School of Information and Electrical Engineering, China University of Mining and Technology, Xuzhou, China
**Department of Energy Technology, Aalborg University, Aalborg, Denmark

Abstract

In recent years, voltage source multilevel converters are very popular in medium/high-voltage industrial applications, among which the NPC/H-Bridge converter is a popular solution to the medium/high-voltage drive systems. The conventional finite control set model predictive control (FCS-MPC) strategy is not practical for multilevel converters due to their substantial calculation requirements, especially under high number of voltage levels. To solve this problem, a hierarchical model predictive voltage control (HMPVC) strategy with referring to the implementation of g-h coordinate space vector modulation (SVM) is proposed. By the hierarchical structure of different cost functions, load currents can be controlled well and common mode voltage can be maintained at low values. The proposed strategy could be easily expanded to the systems with high number of voltage levels while the amount of required calculation is significantly reduced and the advantages of the conventional FCS-MPC strategy are reserved. In addition, a HMPVC-based field oriented control scheme is applied to a drive system with the NPC/H-Bridge converter. Both steady-state and transient performances are evaluated by simulations and experiments with a down-scaled NPC/H-Bridge converter prototype under various conditions, which validate the proposed HMPVC strategy.

Key words: NPC/H-Bridge converter, model predictive control (MPC), common mode voltage elimination, computational burden reduction

I. INTRODUCTION

Multilevel voltage source converter (VSC) topologies are widely researched in recent years [1]. Due to their multistep output voltages and large numbers of switching devices, they exhibit better power quality, lower switching frequency, lower switching device rating, smaller voltage jump \(dv/dt\) and flexible redundant configurations. These advantages make these multilevel converters become very popular and efficient solutions to medium/high-voltage and high-power applications [2]-[9]. They have been widely employed in high-power drives [2], [3], high-voltage direct-current (HVDC) transmissions [4], [5], active power filters (APF) [6], static synchronous compensators (STATCOM) [7] and other industrial applications [8], [9] in the past decades.

Among the various multilevel converters, the neutral point clamped (NPC) and the cascaded H-Bridge (CHB) are the two widely used and well-established topologies very suitable for medium-voltage high-power drives up to now [10], [11]. With the three-level NPC, the drive systems can easily achieve high performances benefiting from its ease of four-quadrant operation under an alternative back-to-back configuration [12]. However, limited by the voltage rating of the available high-power switching devices, the three-level NPC is mostly applied in commercial applications with line-to-line output voltages below 6 kV, such as drive systems with 3.3 kV and 4.16 kV output voltages. The CHB topology will be much more suitable if higher output voltages are required, as higher number of voltage levels could be easily acquired due to its cascaded and modular structure [13]. The NPC/H-Bridge converter was proposed in the late 1990s by combining the NPC and CHB topologies and then applied
in industrial drive applications [14], [15], such as the ACS 5000 Medium Voltage Drive manufactured by ABB, with output voltage and power ranging from 6 kV-13.8 kV and 5 MW-36 MW, respectively [16]. The topology of the five-level NPC/H-Bridge converter is shown in Fig. 1. Similar to the CHB converter, it usually consists of phase-shifting transformers along with multi-pulse diode rectifiers to supply the dc voltages \( V_{a1} \) to \( V_{c2} \) for the H-Bridges.

![Fig. 1. Topology of the five-level NPC/H-Bridge converter](image)

A main research point of the NPC/H-Bridge converters is about the pulse width modulation (PWM) techniques. The modulation algorithm commonly used in commercial applications is multilevel sinusoidal-PWM (SPWM) [17]. The space vector modulation (SVM) is also considered for the modulation of NPC/H-Bridge converters to improve the utilization of dc voltage. However, it is difficult to implement the SVM for the NPC/H-bridge topology with five or higher voltage levels since the math calculation of duty cycles is very heavy. To address this matter, various methods have been introduced to reduce the computation of the SVM applied in multilevel converters [18]-[21]. In addition, a novel switching sequence is designed in [22] to improve the output voltage spectrum and minimize the switching frequency for the five-level NPC/H-Bridge converter.

The control schemes for the NPC/H-Bridge converter based drive system with the PWM techniques above, such as the field oriented control (FOC) and direct torque control (DTC) [23], are mostly with PI controllers. The control parameters of such controllers are difficult to design and adjust, thus the performance of the systems could be influenced if the control parameters are non-optimal. The model predictive control (MPC) is a discrete-model based algorithm especially suitable for non-linear multi-input-multi-output (MIMO) systems. When compared with the conventional linear controllers based schemes, the MPC-based scheme owns advantages such as simple system design, ease of handling multiple control objectives, flexible constrain limits and high dynamic performance, etc [24]. In the past decade, the finite control set MPC (FCS-MPC) strategies have drawn lots of interests in the field of power electronics and electrical drives [24]. It is an innovative manner to adopt the MPC algorithm in the control of the nonlinear and discontinuous power converters. Fig. 2 shows the basic control principle of the FCS-MPC strategies for power converters. As seen, the implementation procedure includes two main steps: variable prediction and rolling optimization.

![Fig. 2. Basic control principle of the FCS-MPC strategies for power converters](image)

The FCS-MPC strategies for conventional two-level converter and three-level NPC converter are designed and introduced in [24]. The load currents at the ac side are with satisfied high dynamic characteristics, which are controlled by the optimal switching state selected from all available switching states by the rolling optimization process based on the load current predictive model. However, a very heavy computational burden will occur when considering FCS-MPC method for the converters with five or higher voltage levels. This is mainly because the sharply increased number of available switching states, e.g., equal to \( N^3 \) (where \( N \) is the number of voltage levels) in the SVM, which must cause the rolling optimization process cost too much execution time. A lot of valuable efforts have been made by researchers with the aim of applying the MPC algorithm to the control of various multilevel converters [25]-[27]. An MPC strategy with consideration of a subset of the available voltage vectors to simplify the rolling optimization process is proposed for the CHB converter in [25]. Satisfied performances with the \( RL \) load are achieved but the performances with ac motors are not introduced. In [26], a fast MPC strategy is designed by combining the voltage sorting algorithm for modular multilevel converters (MMC), which is especially suitable for the applications with large numbers of submodules, such as HVDC transmission. This strategy is based on the independent control of each phase in the converter, thus the utilization of dc voltage is lower when compared to the FCS-MPC strategies based on voltage space vectors. A FCS-MPC strategy for flying-capacitor converters (FCC) is implemented with the FPGA in [27], by which the rolling optimization process can be executed in parallel, but still lacks of practicability in the term of hardware resource deficiency. Up to now, to the authors’ best knowledge, no attempt has been made to apply MPC algorithm for the NPC/H-Bridge converters, especially for its applications of high power motor drives.

In this paper, a hierarchical model predictive voltage control (HMPVC) strategy is proposed for the NPC/H-Bridge converters with any voltage levels. Significant reduction of the computational burden in the proposed strategy is achieved.
from two aspects. Firstly, the voltage prediction is carried out instead of the current prediction in the variable prediction process. This goal is achieved by establishing the load model of ac side. Secondly, the rolling optimization is simplified by combining the implementation of g-h coordinate SVM which can reduce the finite control set from all available base voltage vectors to the ones nearest to the predicted reference voltage vector. Thus the number of rolling times is only three during each sampling period. In addition, the HMPVC strategy is applied to the field oriented control for the NPC/H-Bridge converter drive system. In this paper, a down-scaled experimental prototype is built to validate the proposed HMPVC strategy in the RL load and the induction motor. Simulations and experiments on different conditions are conducted with steady-state and transient performance evaluated and discussed in detail.

The rest of this paper is structured as follows. In Section II, the mathematical load model of the NPC/H-bridge converter is derived and the HMPVC strategy is designed. Section III presents the analysis and improvement of the HMPVC strategy by simulations with RL load. Furtherly, the HMPVC-FOC scheme is evaluated by simulation studies in Section IV. Then, an experimental prototype and experimental results are shown in Section V, followed by conclusions in Section VI.

II. BASIC DESIGN OF THE HMPVC STRATEGY

A. Conventional FCS-MPC strategy for the NPC/H-bridge converter

According to the design procedure of FCS-MPC strategy introduced in [24], the load current dynamic of the NPC/H-bridge converter shown in Fig. 1 in the α-β reference frame can be expressed as

\[ v_{\alpha, \beta} = R i_{\alpha, \beta} + L \frac{di_{\alpha, \beta}}{dt} \]  

(1)

where \( v_{\alpha, \beta} \) and \( i_{\alpha, \beta} \) are the output voltage vector and load current vector with the α-β coordinate, respectively.

Considering that the sampling period \( T_s \) is extremely short, the mathematical model can be discretized by the Euler forward equation. Then the discrete-domain dynamic expression of the load currents can be described as

\[ i_{\alpha, \beta}^{*}(k+1) = \left(1 - \frac{R T_s}{L}\right) i_{\alpha, \beta}(k) + \frac{T_s}{L} v_{\alpha, \beta}(k) \]  

(2)

Based on the predicted results by the load current model above, then the optimal switching state of each time step can be achieved by evaluating the cost function defined as follows.

\[ g = |i_{\alpha}^{*}(k+1) - i_{\alpha}^{\beta}(k+1)| + |i_{\beta}^{*}(k+1) - i_{\beta}^{\alpha}(k+1)| \]  

(3)

where \( i_{\alpha}^{*}(k+1) \) and \( i_{\beta}^{*}(k+1) \) are the real part and imaginary part of the predicted load current vector \( i_{\alpha, \beta}^{*}(k+1) \), while \( i_{\alpha}^{\beta}(k+1) \) and \( i_{\beta}^{\alpha}(k+1) \) are the real part and imaginary part of the reference load current vector \( i_{\alpha, \beta}^{\beta}(k+1) \), respectively.

The space vector diagram for the five-level NPC/H-bridge converter is shown in Fig. 3. As seen, there are 125 available switching states in total and 61 different base voltage vectors. To select the optimal switching state with the FCS-MPC strategy, the rolling optimization process will calculate (2) and (3) for each switching states. Obviously, this process needs large amounts of calculation within each sampling period, making it occupy too much computational burden in the overall control strategy. The rolling optimization process of the strategy was tested on a DSP control platform, the actual runtime being about 0.1 ms for the total 125 switching states and nearly 50 μs for the 61 different base voltage vectors. As known, the sampling period should be larger than these runtimes in the actual implementation because the control strategy includes some other necessary parts, which also need calculation resources. Moreover, the control period should be set as small as possible (usually smaller than 0.1 ms) to ensure the load current control performance. Hence the conventional FCS-MPC strategy is inappropriate to be implemented for the NPC/H-bridge converters with the commonly-used digital controller platforms. To improve the practicability of applying MPC algorithm to the control of NPC/H-bridge or the other multilevel converters, the calculation of implementing the MPC algorithm should be reduced with specific approaches.

Fig. 3. Space voltage vector diagram for the five-level NPC/H-bridge converter

B. Basic design of the HMPVC strategy for the NPC/H-bridge converter

The main problem of the conventional FCS-MPC strategy is that the number of rolling times in the rolling optimization process is too large, as a result of the numerous available switching states of multilevel converters. Hence if the alternative base voltage vectors during each sampling period are limited appropriately, the heavy computational burden will be reduced. The HMPVC strategy proposed in this paper is to reduce the heavy computational burden to a large extent. Unlike the conventional FCS-MPC strategy, which determine the optimal switching state with load current predictive model, the HMPVC strategy utilizes the voltage predictive model to acquire predicted reference voltage vector, and then the optimal switching state is finally determined by combining
the implementation procedure of the $g$-$h$ coordinate (60 degree coordinate) SVM. The basic design of the HMPVC strategy is introduced in detail as follows.

The following four steps should be carried step by step in each sampling period to implement the HMPVC strategy:

Step 1: prediction of the reference voltage vector;
Step 2: handling of over modulation;
Step 3: selection of the optimal base voltage vector;
Step 4: generation of the optimal switching state.

1) Prediction of the reference voltage vector: The reference voltage vector can be predicted by mathematical model of the HMPVC strategy derived based on the load model expressed in (1) and Euler forward equation as follows.

$$v_{ref \alpha, \beta}^{p}(k+1)=Ri_{\alpha, \beta}(k)+L\frac{\dot{i}_{\alpha, \beta}(k+1)-\dot{i}_{\alpha, \beta}(k)}{T_s} \tag{4}$$

where $v_{ref \alpha, \beta}^{p}(k+1)$ is the predicted reference voltage vector, and $i_{\alpha, \beta}(k+1)$ is the load current vector which is expected to be equal to $i_{\alpha, \beta}(k+1)$. The commonly used Second-order Lagrange extrapolation formula as shown in (5) is adopted to obtain the reference load current for the proposed HMPVC strategy.

$$i_{\alpha, \beta}(k+1) \approx 3i_{\alpha, \beta}(k)-3i_{\alpha, \beta}(k-1)+i_{\alpha, \beta}(k-2) \tag{5}$$

2) Handling of overmodulation problem: The reference voltage vector predicted in Step 1 may exceed the range of the hexagon modulation region shown in Fig. 3 and this overmodulation problem should be settled. The optimization strategy of the overmodulation is not included in this paper due to the limited space. Nevertheless, with the aim of making the HMPVC strategy achieve similar performance in controlling the load currents to the conventional FCS-MPC strategy, a simple method is designed for handling the overmodulation problem in this paper, which can be described by Fig. 4 and equation (6).

$$\begin{align*}
  v_{ref \alpha, \beta} &= v_{ref \alpha, \beta}^p, \\
  v_{ref \alpha, \beta} &= \begin{cases} 
  v_{ref \alpha, \beta}^p, & v_{ref \alpha, \beta}^p \leq v_{max \alpha, \beta}^p \\
  \frac{2V_d}{\sqrt{3}\cos(\pi/6-\phi_0)}, & v_{ref \alpha, \beta}^p > v_{max \alpha, \beta}^p
  \end{cases}
\end{align*} \tag{6}$$

where $v_{max \alpha, \beta}^p$ is the available maximum voltage vector, $v_{ref \alpha, \beta}$ is the final reference voltage vector after overmodulation handling process, $\phi$ is the vector angle in the $\alpha$-$\beta$ reference and $\phi_0$ is the vector angle in each sector separated by every 60 degree.

3) Selection of the optimal base voltage vector: In this paper, the rolling optimization process in the HMPVC strategy is simplified by reducing the number of rolling times of rolling optimization to make it easier for the control of the five-level NPC/H-bridge converters. This is achieved by only considering the nearest base voltage vectors around the reference voltage vector for the rolling optimization. The reference voltage vector will be within the hexagon modulation region shown in Fig. 3 after step 2 and then the nearest base voltage vectors can be determined by the $g$-$h$ coordinate SVM method. Firstly, the reference voltage vector expressed in the $\alpha$-$\beta$ coordinate should be transformed to the $g$-$h$ coordinate by the following transformation as

$$\begin{pmatrix}
  v_{\text{ref } g} \\
  v_{\text{ref } h}
\end{pmatrix} = \begin{pmatrix}
  1 & -1/\sqrt{3} \\
  0 & 2/\sqrt{3}
\end{pmatrix} \begin{pmatrix}
  v_{ref \alpha} \\
  v_{ref \beta}
\end{pmatrix} \tag{7}$$

where $v_{\text{ref } g}$ and $v_{\text{ref } h}$ are the axis values of the $v_{\text{ref } \alpha, \beta}$expressed in the $g$-$h$ coordinate, while $v_{\text{ref } \alpha}$ and $v_{\text{ref } \beta}$ are the axis values expressed in the $\alpha$-$\beta$ coordinate, respectively.

Then the nearest four base voltage vectors as the endpoints of the quadrangle around the reference voltage vector $v_{\text{ref } \alpha, \beta}$ can be easily obtained by the following equations given in (8).

$$\begin{align*}
  v_{ul} &= \begin{cases} 
  \text{ceil}(v_{\text{ref } g}), & v_{lu} = \begin{cases} 
  \text{floor}(v_{\text{ref } g}), & v_{uu} = \begin{cases} 
  \text{ceil}(v_{\text{ref } h}), & v_{ll} = \begin{cases} 
  \text{floor}(v_{\text{ref } g}), & v_{ul} = \begin{cases} 
  \text{ceil}(v_{\text{ref } h}), & v_{uu} = \begin{cases} 
  \text{floor}(v_{\text{ref } g}), & \text{floor}(v_{\text{ref } h})
  \end{cases}
  \end{cases}
  \end{cases}
  \end{cases}
  \end{cases}
\end{align*} \tag{8}$$

where ceil($x$) and floor($x$) are the round-up integer function and round-down integer function, respectively.

In this manner, the number of base voltage vectors for consideration in each sampling period can be reduced from 61 to 4. Nevertheless, this number can be reduced to only three for further reduction of the computational burden of the HMPVC strategy. By observing the four base voltage vectors above shown in Fig. 5, it is obvious that $v_{ul}$ and $v_{lu}$ are the most two nearest base voltage vectors (represented by $v_1$ and $v_2$ below) and then the third one can be determined by judging the sign of $[v_{ref g} + v_{ref h} - (v_{ud g} + v_{ud h})]$, where $v_{ud g}$ and $v_{ud h}$ are the axis values of $v_{ul}$ in the $g$-$h$ coordinate. The third nearest base voltage vector $v_3$ will be $v_{uu}$ if the sign is positive, otherwise it will be $v_{ll}$ if the sign is negative.

The rolling times of the rolling optimization process in each sampling period will be finally reduced to three, which is small enough to be implemented for multilevel converters. Hence the HMPVC algorithm can be expediently extended to higher voltage levels without the restriction resulted from the computational burden. To select the optimal voltage vector
(represented by $v_{opt}$ below) for current sampling period, the first-stage cost function is defined as (9) and the base voltage vector with the smallest cost function value will be set as $v_{opt}$ for the present sampling period.

$$g(i) = |v_{ref,g} - v_{i,g}| + |v_{ref,h} - v_{i,h}|$$  \hspace{1cm} (9)

where $i$ and $g(i)$ are the mark number and corresponding cost function value of the three nearest base voltage vectors ($v_1$, $v_2$ and $v_3$), respectively. $v_{i,g}$ and $v_{i,h}$ are the axis values of these vectors in the $g$-$h$ coordinate.

For the conventional FCS-MPC, with the aim of determining the optimal base voltage vector, the predicted current vectors related to all of the base voltage vectors (with the number being at least 61 for a five-level converter) need to be calculated and compared to the certain reference current based on equation (3) in each sampling period. Unlike the conventional FCS-MPC, the proposed HMPVC employs voltage predictive model instead of current predictive model in the rolling optimization process. Since the reference current vector is certain, the only reference voltage vector of the HMPVC can be predicted directly on the basis of the current vector control requirement by the voltage predictive model shown in equation (4). From the perspective of mathematics, it is obvious that the base vectors which closest to the predicted reference voltage vector will make the value of equation (9) smallest, and it will be the optimal base voltage vector certainly. Hence only the base voltage vectors surround the base voltages are need to be evaluated for the HMPVC strategy.

4) Generation of the optimal switching state: According to the space voltage vector diagram shown in Fig. 3, it can be seen that a base voltage vector may correspond to several switching states. In the $g$-$h$ coordinate, all the relative switching states of the selected optimal voltage vector $v_{opt}$ can be obtained by the equations as follows.

$$S_x(j) = j$$

$$S_x(j) = j - v_{opt,g} \text{, and } -2 \leq j \leq 2$$

$$S_x(j) = j - v_{opt,g} - v_{opt,h} \text{, and } -2 \leq j \leq v_{opt,g} - v_{opt,h} \leq 2$$  \hspace{1cm} (10)

where $j \in \{-2,-1,0,1,2\}$, $S_x$ is the switching function of phase-$x$ ($x=a$, $b$, $c$), $v_{opt,g}$ and $v_{opt,h}$ are the axis values of the optimal voltage vectors in the $g$-$h$ coordinate, respectively.

The principle for selecting the optimal switching state for present sampling period from all the relative switching states of $v_{opt}$ is to reduce common mode voltage (denoted by "$v_{com}$") as much as possible. Then the optimal switching state for current sampling period can be determined by judging the following second-stage cost function in the hierarchical control system:

$$J(j) = |S_a(j) + S_b(j) + S_c(j)|$$  \hspace{1cm} (11)

The switching state which owns the smallest value of $J$ will be set as the optimal switching states for current sampling period. Obviously, in the HMPVC strategy, the first-stage cost function is to achieve the goal of tracking load currents, and the second-stage cost function is established to reduce common mode voltage.

The basic design of the HMPVC strategy introduced above avoids large amount of calculation by the voltage predictive model and $g$-$h$ coordinate SVM algorithm. In addition, the calculation time delay should also be taken into account in the real implementation with the digital controllers, the compensation method will be introduced in the next section.

III. ANALYSIS AND IMPROVEMENT OF THE PROPOSED HMPVC STRATEGY

With the aim of improving the basic design of the HMPVC strategy for the NPC/H-bridge converters further and investigating its robustness characteristic, simulations under various conditions are carried out with the MATLAB/Simulink software and the corresponding results are evaluated. The simulated model is constructed based on the configuration shown in Fig. 1 with a three-phase resistance and inductance (RL) load and the simulation parameters are shown in Table I. The simulation analysis is mainly about the following two aspects: (1) verification on the compensation method of the time delay; and (2) robustness of the HMPVC strategy.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_s$</td>
<td>Peak value of reference load currents</td>
<td>25 A</td>
</tr>
<tr>
<td>$f$</td>
<td>Frequency of load currents</td>
<td>50 Hz</td>
</tr>
<tr>
<td>$V_{dc}$</td>
<td>Supplied dc-link voltage for each</td>
<td>150 V</td>
</tr>
<tr>
<td>$C$</td>
<td>Capacitance of the dc-link capacitors</td>
<td>2200 μF</td>
</tr>
<tr>
<td>$R$</td>
<td>Load Resistance</td>
<td>10 Ω</td>
</tr>
<tr>
<td>$L$</td>
<td>Load inductance</td>
<td>9 mH</td>
</tr>
<tr>
<td>$T_s$</td>
<td>Sampling period</td>
<td>100 μs</td>
</tr>
</tbody>
</table>

A. Verification on the compensation method of the time delay

In the digital control systems for multilevel converters, the calculation time is usually significant when compared to the sampling period, and the switching states are commonly applied at the beginning of the next sampling instant. In the MPC strategies, the switching states generated for time step $k+1$ will be applied at the beginning of time step $k+2$ [24]. Since the HMPVC strategy achieves the control target by predicting the reference voltage rather than the reference current, the delay compensation method introduced in [24] for conventional FCS-MPC strategies is no more suitable.

In the HMPVC strategy, the reference voltage vector obtained by equation (4) is on the basis of the sampled actual load current vector and obtained reference current vector for present time step. However, the optimal switching state generated based on the reference voltage vector for present time step will be applied at the beginning of next time step. This will influence the load current control performance since the necessary reference current vector of present time step will no longer be accurate enough for next time step. Thus,
the reference current vector should be calculated with equation (5) by one more iteration for next time step. Thus to compensate the delay for the proposed HMPVC strategy, the prediction model in (4) is modified as (12), which could help to reduce the control error by predicting the reference voltage vector at time step \( k+2 \).

\[
v^p_{\text{ref}, \alpha, \beta}(k+2) = Ri_{\alpha, \beta}(k) + \frac{L}{2T_s} (i^*_{\alpha, \beta}(k+2) - i_{\alpha, \beta}(k)) \quad (12)
\]

Corresponding simulation results of the delay compensation method are shown in Fig. 6. Fig. 6(a) and Fig. 6(b) are the waveforms and total harmonic distortion (THD) analysis of phase-a load current without the delay compensation method, respectively. Fig. 6(c) and Fig. 6(d) are the waveforms and THD analysis of phase-a load current with the delay compensation method, respectively. As can be seen, in Fig. 6(a) the waveform of the actual load current \( i_a \) lags behind its reference value \( i^*_a \) to some degree without the delay compensation method. This is mainly because the delayed time makes the error of \( i^*_a \), and then the predicted reference voltage vector will be not accuracy. However, the lag in Fig. 6(c) is smaller with the designed delay compensation method, and the THD of the load current is reduced from 4.13% to 3.74%. Hence the effectiveness of the proposed delay compensation method is verified based on the simulation results. All the simulation and experimental studies in this paper will cover this method for a better performance.

![Fig. 6](image)

**Fig. 6. Simulation results of the delay compensation method:** (a) Phase-a load current waveforms without delay compensation method. (b) THD analysis of Phase-a load current without delay compensation method. (c) Phase-a load current waveforms with delay compensation method. (d) THD analysis of Phase-a load current with delay compensation method.

### B. Robustness of the HMPVC strategy

The reference parameters of inductance and the resistance of the \( RL \) load used in the predictive model are set with ±80% deviations to evaluate the robustness of the HMPVC strategy. The simulation results of the reference inductance deviations and reference resistance deviations are shown in Fig. 7 and Fig. 8, respectively.

Fig. 7(a) and Fig. 7(b) are the waveforms and THD analysis of phase-a load current with \( L^* = 0.2L \) as the reference parameter of load inductance, respectively. There is a significant lag between \( i_a \) and \( i^*_a \), and the THD is much larger than the simulation result of normal condition shown in Fig. 6(d). Fig. 7(c) and Fig. 7(d) are the waveforms and THD analysis of phase-a load current with \( L^* = 1.8L \) as the reference parameter of load inductance, respectively. As seen, the phase position in this condition is controlled well. However, the harmonics around 20th order in the load current become larger according to Fig. 7(d), which make the THD also increase to 4.75% from 3.74%.

![Fig. 7](image)

**Fig. 7. Simulation results of the reference inductance deviations:** (a) Phase-a load current waveforms with \( L^* = 0.2L \). (b) THD analysis of Phase-a load current with \( L^* = 0.2L \). (c) Phase-a load current waveforms with \( L^* = 1.8L \). (d) THD analysis of Phase-a load current with \( L^* = 1.8L \).

Fig. 8(a) and Fig. 8(b) are the waveforms and THD analysis of phase-a load current with \( R^* = 0.2R \) as the reference parameter of load resistance, respectively. Fig. 8(c) and Fig. 8(d) are the waveforms and THD analysis of phase-a load current with \( R^* = 1.8R \) as the reference parameter of load resistance, respectively. Obviously, the phase positions in these two conditions are controlled well, along with the THD being even smaller than the simulation results of normal condition in Fig. 6(c) and (d). Nevertheless, the actual load current deviates from its reference value to some degree as a result of the deviations on reference parameter of resistance. Larger reference parameter of resistance causes larger actual load current, vice versa.

![Fig. 8](image)

**Fig. 8. Simulation results of the reference resistance deviations:** (a) Phase-a load current waveforms with \( R^* = 0.2R \). (b) THD analysis of Phase-a load current with \( R^* = 0.2R \). (c) Phase-a load current waveforms with \( R^* = 1.8R \). (d) THD analysis of Phase-a load current with \( R^* = 1.8R \).
current waveforms with $R^* = 1.8R$. (d) THD analysis of Phase-a load current with $R^* = 1.8R$.

IV. CONTROL OF A DRIVE SYSTEM BASED ON THE NPC/H-BRIDGE CONVERTER WITH HMPVC STRATEGY

A. Introduction of the control scheme with induction motors

The main control objective of the HMPVC strategy presented in Section II and Section III is the load currents control of the NPC/H-Bridge converter. Thus the inner current loops with PI controllers in the conventional field oriented control (FOC) scheme for motor drives can be replaced by the HMPVC strategy, with the aim of getting rid of the complex design and adjusting procedure of the PI controllers. In addition, a better dynamic performance is expected to be achieved benefiting from the HMPVC strategy. The block diagram of the HMPVC-based FOC (HMPVC-FOC) scheme is illustrated in Fig. 9.

The classical rotor flux observer based on the current model [28] is adopted for the control scheme to obtain the rotor flux and stator angle in this paper. The HMPVC controller in the HMPVC-FOC scheme is based on the discrete load model of the power converter with an induction motor (IM) to predict the reference voltage vector. Only the Step 1 in Section II-B needs to be designed again as below.

According to the dynamic characteristic of the induction motors, the voltage model for the commonly used FOC scheme can be deduced as:

$$\begin{align*}
    v_{sM} &= \sigma L_s \frac{di_{sM}}{dt} + \frac{R_t L_r^2 + R_m L_m^2}{L_r^2} i_{sM} - \frac{L_m \psi_r}{L_r T_r} - \omega \frac{L_m \psi_r}{L_r} \sigma L_s, \\
    v_{sT} &= \sigma L_s \frac{di_{sT}}{dt} + \frac{R_t L_r^2 + R_m L_m^2}{L_r^2} i_{sT} + \frac{L_m \omega \psi_r}{L_r} + \omega \frac{L_m \sigma L_s}{L_r}
\end{align*}$$

(13)

Then this voltage model can be discretized with the Euler forward equation as:

$$\begin{align*}
    v_{sM}(k+1) &= \sigma L_s \frac{i_{sM}(k+1) - i_{sM}(k)}{T_s} + \frac{R_t L_r^2 + R_m L_m^2}{L_r^2} i_{sM}(k) - \frac{L_m \psi_r}{L_r T_r} - \omega \frac{L_m \psi_r}{L_r} \sigma L_s, \\
    v_{sT}(k+1) &= \sigma L_s \frac{i_{sT}(k+1) - i_{sT}(k)}{T_s} + \frac{R_t L_r^2 + R_m L_m^2}{L_r^2} i_{sT}(k) + \frac{L_m \omega \psi_r}{L_r} + \omega \frac{L_m \sigma L_s}{L_r}
\end{align*}$$

(14)

Thus the reference voltage vector $v_{sM,T}(k+1)$ is predicted in the well-known M-T coordinate and it can be transformed to the $\alpha\beta$ coordinate as $v_{s,\alpha,\beta}(k+1)$ by the park transformation.

For the HMPVC strategy in the drive application, the voltage model for the commonly used FOC scheme can be deduced as:

$$\begin{align*}
    v_{sM} &= \sigma L_s \frac{di_{sM}}{dt} + R_t L_r^2 i_{sM} - \frac{L_m \psi_r}{L_r T_r} - \omega \frac{L_m \psi_r}{L_r} \sigma L_s, \\
    v_{sT} &= \sigma L_s \frac{di_{sT}}{dt} + R_t L_r^2 i_{sT} + \frac{L_m \omega \psi_r}{L_r} + \omega \frac{L_m \sigma L_s}{L_r}
\end{align*}$$

(15)

in Section II-B is set as $v_{s,\alpha,\beta}(k+1)$ to control the stator currents of the induction motors, then the following introduced steps and the delay compensation method will be carried out to generate the optimal switching state for the NPC/H-Bridge multilevel converter.

![Fig. 9. Block diagram of the HMPVC-FOC scheme](image)

B. Simulation study of the HMPVC-FOC scheme

To evaluate the control performances of the HMPVC-FOC scheme, a simulation study on the five-level NPC/H-Bridge converter feeding an IM is carried out and relative simulation results are analyzed. The control system is built up based on Fig. 9, and the parameters of the simulation study are listed in Table II.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{dcl}$, $V_{ac}$</td>
<td>Supplied dc voltage for each H-Bridge</td>
</tr>
<tr>
<td>$C$</td>
<td>Capacitance of the dc-link capacitors</td>
</tr>
<tr>
<td>$P_r$</td>
<td>Rated power of the IM</td>
</tr>
<tr>
<td>$v_s$</td>
<td>Rated voltage of the IM</td>
</tr>
<tr>
<td>$i_s$</td>
<td>Rated current of the IM</td>
</tr>
<tr>
<td>$t_s$</td>
<td>Rated current of the IM</td>
</tr>
<tr>
<td>$J_s$</td>
<td>Rated frequency of the IM</td>
</tr>
<tr>
<td>$R_r$</td>
<td>Stator resistance of the IM</td>
</tr>
<tr>
<td>$R_s$</td>
<td>Rotor resistance of the IM</td>
</tr>
<tr>
<td>$L_s$</td>
<td>Stator inductance of the IM</td>
</tr>
<tr>
<td>$L_r$</td>
<td>Rotor inductance of the IM</td>
</tr>
<tr>
<td>$J$</td>
<td>Rotational inertia of the IM</td>
</tr>
<tr>
<td>$\psi_r$</td>
<td>Reference rotor flux of the IM</td>
</tr>
<tr>
<td>$n_r$</td>
<td>Rated speed of the IM</td>
</tr>
<tr>
<td>$T_s$</td>
<td>Sampling period</td>
</tr>
</tbody>
</table>

In the simulation study, the reference rotor speed is set as 1000 rpm at 0 s, then steps to 500 rpm at 0.4 s and 1300 rpm at 0.6 s, respectively. The load torque is set as zero from 0 s to 1 s, and then steps to 10 N.m at 1 s and 20 N.m at 1.2 s, respectively. In addition, the maximum outputs of the two PI controllers are limited to 15 A to protect the motor with consideration of the practical applications. Fig. 10 illustrates the simulation results of this simulation study case. Fig. 10(a) and Fig. 10(b) show the simulation waveforms of the rotor speed and electromagnetic torque, respectively. Fig. 10(c) shows the simulation waveforms of the three-phase stator currents while Fig. 10 (f) shows the partial enlarged
waveforms. Fig. 10(d) shows the simulation waveform of the line-to-line voltage between phase-\(a\) and phase-\(b\) while Fig. 10(f) shows the partial enlarged waveform. As can be seen in Fig. 10(a) and Fig. 10(b), both the rotor speed and electromagnetic torque achieve satisfied steady-state performances. The electromagnetic torque has fast responses when the load torque changes with steps, and the rotor speed varies very tiny and can be regulated to its reference speed quickly. The stator currents in Fig. 10(c) and Fig. 10(e) further verify that the HMPVC-FOC scheme can achieve a high dynamic-state performance since the currents response very quickly to track their reference values when the reference rotor speed or the load torque steps. It can be conducted that the high dynamic performance of the conventional FCS-MPC strategy is remained by the proposed HMPVC strategy while the computational burden is notably reduced. According to the simulation waveforms in Fig. 10(d) and Fig. 10(f), it can be seen that the maximum number of the line-to-line voltage levels is nine, which is coincide with the expectation of design. Fig. 10(e) shows the waveform of common mode voltage, which is maintained in low voltage levels with its peak-to-peak values almost being about 107 V in the whole simulation study.

Fig. 10. Simulation results of the NPC/H-Bridge converter drive system based on the HMPVC-FOC scheme. (a) Rotor speed performance of the IM. (b) Electromagnetic torque characteristic of the IM. (c) Three-phase stator currents of the IM. (d) Line-to-line voltage between phase-\(a\) and phase-\(b\). (e) Common mode voltage. (f) Partial enlarged waveforms of (c). (g) Partial enlarged waveform of (d).

A comparative simulation study of the drive system with the conventional FCS-MPC strategy has also been carried out to show the advantage of the proposed HMPVC strategy. In this simulation study, the conventional FCS-MPC-based FOC (FCS-MPC-FOC) scheme of the drive system is designed in \(\alpha-\beta\) coordinate which considering all possible 125 switching states of the five-level NPC/H-Bridge converter. All simulation conditions and parameters are same with the ones of the simulation study shown in Fig. 10. Relative simulation results are shown in Fig. 11. As can be seen in Fig. 11(a) and Fig. 11(b), the characteristics of the rotor speed and electromagnetic torque with the conventional FCS-MPC strategy are exactly similar to the ones with the proposed HMPVC strategy. This is mainly because the current control performance of the HMPVC strategy is very closed to the conventional FCS-MPC, both from the perspectives of
steady-state [seen in Fig. 10(c) and Fig. 11(c)] and dynamic-state [seen in Fig. 10(f) and Fig. 11(f)]. Since the conventional FCS-MPC strategy is implemented by considering all possible switching states without the consideration of reducing common mode voltage, the pulse patterns of these two strategy are different to some degree. This can be verified by the delicate difference between the simulation results of the line-to-line voltage shown in Fig. 10(d)/(g) and Fig. 11(d)/(g), and the obvious difference between the results of the common mode voltage shown in Fig. 10(e) and Fig. 11(e). Hence the HMPVC strategy reserves the advantages of the conventional FCS-MPC strategy while the computational burden and the common mode voltage are significantly reduced.

V. EXPERIMENTAL RESULTS

A. Experimental results of the HMPVC strategy with the RL load

In this part, experiments with the RL load are carried out with corresponding to two aspects of simulation analysis in Section III. In addition, the control effectiveness of load current’s dynamic-state performance is also evaluated. The parameters of these experiments with the RL load are listed in Table III.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I^*$</td>
<td>Peak value of reference load currents</td>
<td>3 A</td>
</tr>
<tr>
<td>$f$</td>
<td>Frequency of load currents</td>
<td>50 Hz</td>
</tr>
<tr>
<td>$V_{x1}, V_{x2}$</td>
<td>Supplied dc-link voltage for each</td>
<td>30 V</td>
</tr>
<tr>
<td>$C$</td>
<td>Capacitance of the dc-link capacitors</td>
<td>2200 μF</td>
</tr>
<tr>
<td>$R$</td>
<td>Load Resistance</td>
<td>15.5 Ω</td>
</tr>
<tr>
<td>$L$</td>
<td>Load inductance</td>
<td>9 mH</td>
</tr>
<tr>
<td>$T_s$</td>
<td>Sampling period</td>
<td>100 μs</td>
</tr>
</tbody>
</table>

Experimental results of the delay compensation method are shown in Fig. 12 with corresponding to the simulation results shown in Fig. 6. As can be seen, the lag between the reference load current ($i_{a}^*$) and actual load current ($\bar{i}_a$) becomes smaller obviously when the proposed delay compensation method is adopted. Meanwhile the THD decreases from 3.1% to 2.2%, which is coincide with the simulation results as well.

Fig. 13 shows the experimental waveforms of the robustness tests about reference inductance for the HMPVC strategy with corresponding to the simulation results shown in Fig. 7. According to Fig. 13(a) and Fig. 13(b), it can be seen with the similar phenomenon in simulation analysis, the $i_a$ lags behind $i_{a}^*$ significantly with $L^*=0.2L$ as the reference parameter of load inductance. Meanwhile the THD is larger than the one of normal condition shown in Fig. 12(d). The difference between the experimental and simulation results is that the actual load current shown in Fig. 13(a) is not controlled very well in the term of tracking its reference load current amplitude. With the experimental results about $L^*=1.8L$ shown in Fig. 13(c) and Fig. 13(d), it can be seen more obvious harmonics around 20th order exist in the load current when compared to the simulation results, but the rules of experimental and simulation results are also generally matched.

Fig. 14 shows the experimental waveforms of the...
robustness tests about reference resistance for the HMPVC strategy with corresponding to the simulation results shown in Fig. 8. A very similar effectiveness of the control is achieved by comparing the experimental and simulation results, both in the conditions of $R^* = 0.2R$ and $R^* = 1.8R$. That is larger reference parameter of resistance brings larger actual load current, vice versa. However, the control errors resulted from the deviations in reference resistance is smaller than the ones in reference inductance.

Fig. 14. Experimental results of the reference resistance deviations: (a) Phase-a load current waveforms with $R^* = 0.2R$. (b) THD analysis of Phase-a load current with $R^* = 0.2R$. (c) Phase-a load current waveforms with $R^* = 1.8R$. (d) THD analysis of Phase-a load current with $R^* = 1.8R$.

According to the simulation and experimental results above, it can be concluded that the time delay in digital control systems is necessary to be compensated to ensure the control precision of load current. Meanwhile, the accuracy of the reference load current in the delay compensation method has influence on the tracking performance of the load current to some degree. In the term of robustness, it can be seen the accuracy of the reference parameters of the model have an direct influence on the control performances. The reference parameters of inductance has a bigger influence on the control precision than that of resistance, because there is a notable phase error in the load current control when the reference parameter is much smaller than the actual one. In general, the proposed HMPVC has gained a satisfactory performance since the reference parameters of the model would not deviate so much as in a normal operation condition.

Fig. 15 shows the comparison experimental results about the execution time of conventional FCS-MPC strategy and the proposed HMPVC strategy for the five-level NPC/H-Bridge converter. The waveforms are output by a GPIO of the DSP processor (TI TMS320F28335). In each interrupt period, the GPIO will output high level voltage signal (3.3 V) if the MPC strategies are under executing. Obviously, the conventional FCS-MPC takes about 95 μs to finish the whole computing while the proposed HMPVC strategy takes only about 19 μs, which indicates that the computational burden is notably reduced.

Fig. 15. Experimental results of the execution time of two MPC strategies: (a) conventional FCS-MPC strategy. (b) proposed HMPVC strategy.

B. Experimental results of the HMPVC-FOC scheme with the induction motor

To verify the validity of the HMPVC-FOC scheme practically, experimental studies with the NPC/H-Bridge converter feeding an induction motor are also carried out. Relative experimental parameters are the same as the parameters of simulation study shown in Table II, with a sampling period being 100 μs as well. The only difference is that the supplied dc voltage for each H-Bridge in these experiments is 100 V resulted from the restrictions of experimental conditions in the laboratory. These dc voltages are supplied by a 12-pulse diode rectifier system.

Relative experimental waveforms are shown in Fig. 16. Fig. 16 (a) illustrates a speed-up process of the IM with no load, which is realized by making the reference rotor speed step from 150 rpm to 650 rpm. As seen in the transient, the rotor current of phase-a responds quickly when the speed-up process starts. Both of the stator current excitation and torque components ($i_s^M$ and $i_s^T$) are control well with satisfactory decoupling, and the rotor speed ($n_r$) increases smoothly to its target. In addition, the IM also operates stably in the stable-state. The rest graphs of Fig. 16 are the experimental waveforms under steady-state of $n_r = 650$ rpm with a load of 20 N.m, where Fig. 16(b) shows rotor flux linkage locus in the $d$-$q$ coordinate, the waveforms of line-to-line voltage and stator current are shown in Fig. 16(c), and the common mode

---

10 Journal of Power Electronics, to be published
A Hierarchical Model Predictive Voltage Control for NPC/H-Bridge Converters with Reduced Computational Burden

VI. CONCLUSIONS

In this paper, a novel HMPVC strategy has been proposed to reduce the heavy computational burden for NPC/H-Bridge converters. The optimizations in the proposed strategy have been attained by carrying out the variable prediction process with voltage model and implementing the rolling optimization process. The line-to-line voltage is regular when compared to the features of the conventional PWM methods, e.g., SPWM and SVM. Meanwhile, the line-to-line voltage is nine-level as well and the common mode voltage is at low values. It can be concluded that the characteristics of these experimental waveforms are coincident with the ones of the simulation results in Fig. 10. The feasibility for practical use of the HMPVC-FOC is demonstrated by the experimental evaluation above.

VI. CONCLUSIONS

In this paper, a novel HMPVC strategy has been proposed to reduce the heavy computational burden for NPC/H-Bridge converters. The optimizations in the proposed strategy have been attained by carrying out the variable prediction process with voltage model and implementing the rolling optimization process with combination of the method of g-h coordinate SVM. Then the HMPVC-FOC scheme has been evaluated for the NPC/H-Bridge converter drive system. Simulations and experiments with a downscale five-level NPC/H-Bridge converter prototype under various operating conditions have indicated that the HMPVC strategy and HMPVC-FOC scheme achieve satisfied effectiveness in the load current control. It has also been demonstrated with the simulation and experimental results that the high dynamic performance is reserved even though the calculation is significantly reduced when compared with the conventional FCS-MPC strategy. Since the HMPVC strategy could suit any number of voltage levels, it can be expediently applied to other topologies of multilevel converters such as the CHB converters and MMCs, which are especially recommended for the applications requiring high voltages.

ACKNOWLEDGMENT

This work was supported in part by the Graduate Student Research and Innovation Program of Jiangsu Province in China under Grant KYLX_1384, in part by the Qinglan Innovation Project of Jiangsu Province in China under Grant 04150020, and in part by the China Scholarship Council.

REFERENCES


The text content is a page from a document that includes references and biographies. Each reference is formatted according to the IEEE citation style. There are also brief biographies and career highlights for individuals associated with the content provided.
electrical drives, multilevel converters, renewable energy generation systems, and power electronics.

**Fujin Deng** received the B. Eng. degree in electrical engineering from China University of Mining and Technology, Jiangsu, China, in 2005, the M. Sc. Degree in electrical engineering from Shanghai Jiao Tong University, Shanghai, China, in 2008, and the Ph.D. degree in energy technology from the Department of Energy Technology, Aalborg University, Aalborg, Denmark, in 2012.

From 2013 to 2015, he was a Postdoctoral Researcher in the Department of Energy Technology, Aalborg University, Aalborg, Denmark. Currently, he is an Assistant Professor in the Department of Energy Technology, Aalborg University, Aalborg, Denmark. His main research interests include wind power generation, multilevel converters, DC grid, high-voltage direct-current (HVDC) technology, and offshore wind farm-power systems dynamics.

**Dong Liu** received the B.Eng. degree and M.Sc. degree in electrical engineering from South China University of Technology, Guangdong, China, in 2008 and 2011 respectively. From 2011 to 2014, he was a R&D Engineer in Emerson Network Power Co., Ltd., China. He is currently working toward the Ph.D. degree in the Department of Energy Technology, Aalborg University, Denmark. His main research interests include renewable energy, multilevel converters, DC grid, and dc/dc converters.

**Zhe Chen** received the B.Eng. and M.Sc. degrees all in Electrical Engineering from Northeast China Institute of Electric Power Engineering, Jilin City, China, MPhil in Power Electronic, from Staffordshire University, England and the Ph.D. degree in Power and Control, from University of Durham, England.

Dr. Chen is a full Professor with the Department of Energy Technology, Aalborg University, Denmark. He is the leader of Wind Power System Research program at the Department of Energy Technology, Aalborg University and the Danish Principle Investigator for *Wind Energy of Sino-Danish Centre for Education and Research*.

His research areas are power systems, power electronics and electric machines; and his main current research interests are wind energy and modern power systems. He has led many research projects and has more than 400 technical publications with more than 10000 citations and h-index of 44 (Google Scholar).

Dr. Chen is an Associate Editor of the IEEE Transactions on Power Electronics, a Fellow of the Institution of Engineering and Technology (London, U.K.), and a Chartered Engineer in the U.K.