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Common-mode Voltage Elimination with an Auxiliary Half-bridge Circuit for Five-level Active NPC Inverters

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Abstract

This paper proposes a novel scheme which can compensate the common-mode voltage (CMV) for five-level active neutral-point clamped (5L-ANPC) inverters, which is based on modifying the space vector pulse width modulation (SVPWM) and adding an auxiliary leg to the inverter. For the modified SVPWM, only the 55 voltage vectors producing low CMV values among the 125 possible voltage vectors are utilized, which varies over the three voltage levels of $-V_{dc}/12$, 0 V, and $V_{dc}/12$. In addition, the compensating voltage, which is injected into the 5L-ANPC inverter system to cancel the remaining CVM through a common-mode transformer (CMT) is generated by the additional NPC leg. By the proposed method, the CMV of the inverter is fully eliminated, while the utilization of the DC-link voltage is not decreased at all. Furthermore, all of the DC-link and flying capacitor voltages of the inverter are well controlled. Simulation and experimental results have verified the validity of the proposed scheme.

Keywords: active neutral-point clamped inverter, common-mode voltage, high-power medium-voltage drives, space vector modulation

I. INTRODUCTION

Multilevel voltage source inverters (VSIs) play an important role in industrial applications since they can handle the medium voltage range with a low total harmonic distortion (THD) [1]–[3]. However, the multilevel VSIs produce common-mode voltage (CMV), which causes leakage currents, bearing currents, and degradation of component insulation. Therefore, a lot of methods have been suggested to reduce or eliminate CMV and its effects [4]–[19].

The countermeasures for CMV can be classified into two categories: modulation techniques and auxiliary circuit methods. One CMV elimination method based on the auxiliary circuit of a complementary-symmetry transistor was proposed for two-level inverters [4], [5], where the CMV of the inverter can be fully cancelled without any deterioration of the DC-link voltage utilization or THD of the output voltage. However, due to the power limit of transistors operating in a linear range, this method is inappropriate for medium-voltage inverters. Furthermore, the common-mode transformer (CMT) in the auxiliary circuit should be designed carefully due to the power dissipation constraint of transistors.

Alternatively, in PWM modulation methods, only some selected voltage vectors are utilized, which can satisfy the requirements for CMV reduction or elimination. In the case of the CMV reduction methods in [6]–[10], only the voltage vectors producing low CMV values are selected. As a result, the peak value of the CMV for the VSI can be reduced to $V_{dc}/6$, while the DC-link voltage utilization is maintained. Meanwhile, in modulation techniques where only the voltage vectors producing zero CMV are utilized [7], [18], [19], the CMV of the inverter can be almost cancelled. However, the THD and switching losses are increased and the DC-link voltage utilization is decreased to 0.866.

A promising inverter topology for medium voltage applications is the 5L-ANPC inverter. This inverter can improve the output voltage performance and reduce the THD and the *dv/dt* [2], [20]. Due to its benefits, the 5L-ANPC inverter has been commercialized [21]. Although, modulation schemes to balance the DC-link capacitor voltages have been suggested [22], [23], CMV elimination has not been considered. In [16] and [17], the CMV of a 5L-ANPC inverter can be reduced to $V_{dc}/4$ and $V_{dc}/12$, respectively, where all of the capacitor voltages in the inverters can still be regulated. However, the CMV cannot be fully eliminated.

On the other hand, an SVPWM method which can completely remove the CMV in 5L-NPC inverters was proposed in [7]. However, in this method, the capacitor voltages of the inverter cannot be controlled and the DC-link voltage utilization is 0.866 only.

In this paper, a novel elimination scheme for the CMV in five-level NPC inverters based on an auxiliary leg is proposed,

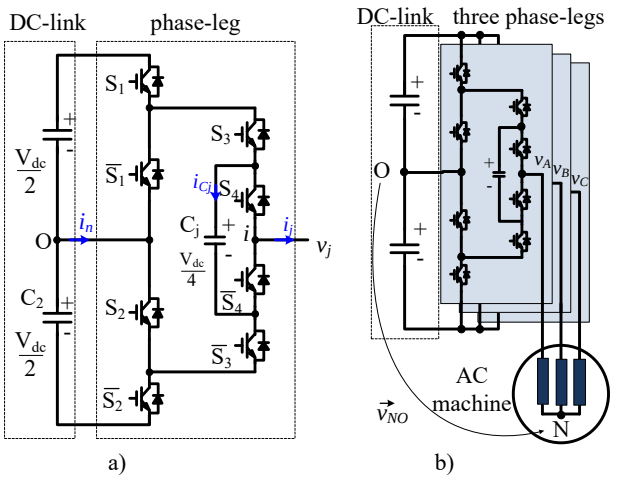

Fig. 1. Five-level ANPC inverters: (a) structure of a phase leg; (b) three-phase 5L-ANPC inverter for an AC machine drive system.

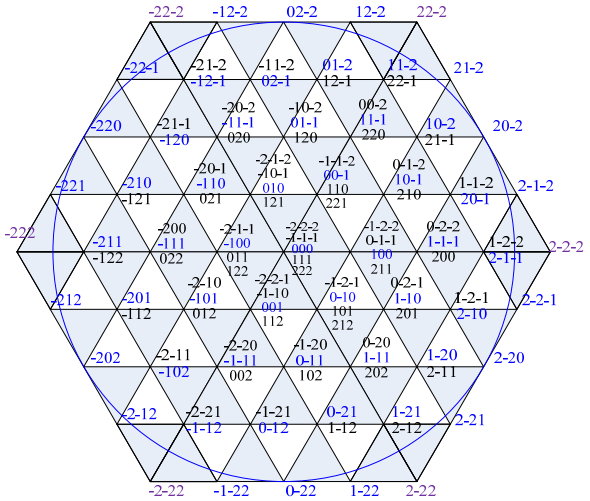

Fig. 2. Conventional space vector diagram of a 5L-ANPC inverter.

TABLE I.

SWITCHING STATES OF 5L-ANPC INVERTERS.

Switching states	v_{jN}	Switching function (S_j)	S_{j1}	S_{j2}	S_{j3}	S_{j4}	i_{Cj}	i_n
V_0	$-V_{dc}/2$	-2	0	0	0	0	0	0
V_1	$-V_{dc}/4$	-1	0	0	0	1	$-i_j$	0
V_2	$-V_{dc}/4$	-1	0	0	1	0	i_j	i_j
V_3	0	0	0	0	1	1	0	i_j
V_4	0	0	1	1	0	0	0	i_j
V_5	$V_{dc}/4$	1	1	1	0	1	$-i_j$	i_j
V_6	$V_{dc}/4$	1	1	1	1	0	i_j	0
V_7	$V_{dc}/2$	2	1	1	1	1	0	0

which consists of a CMT and a low power NPC converter leg. In this method, the maximum modulation index of the inverter is not decreased. The validity of the proposed method is verified by results obtained from simulations of a high power 5L-ANPC inverter and experimental carried out on a hardware prototype in the laboratory.

II. FIVE-LEVEL ANPC INVERTERS

A. Structure of a 5L-ANPC inverter

A phase leg of a 5L-ANPC inverter is composed of eight switches and one flying capacitor. In addition, two DC-link capacitors are connected in series, which are common for three phases of the inverter, as shown in Fig. 1 [2], [20]. It is noted that the rated voltage of the switches S_1 and S_2 and the DC-link capacitors C_1 and C_2 is half the DC-link voltage, $V_{dc}/2$. Meanwhile, that of the other components S_3, S_4, and C_{fly} is only a quarter of the DC-link voltage, $V_{dc}/4$. The higher-voltage-rated switches, S_1 and S_2, are controlled to be operated at a fundamental switching frequency to decrease the switching losses. There are four complementary switch pairs as follows: S_1 and $\overline{S}_1$, S_2 and $\overline{S}_2$, S_3 and $\overline{S}_3$, S_4 and $\overline{S}_4$.

B. Operating Principle

A phase leg of a 5L-ANPC inverter can generate eight

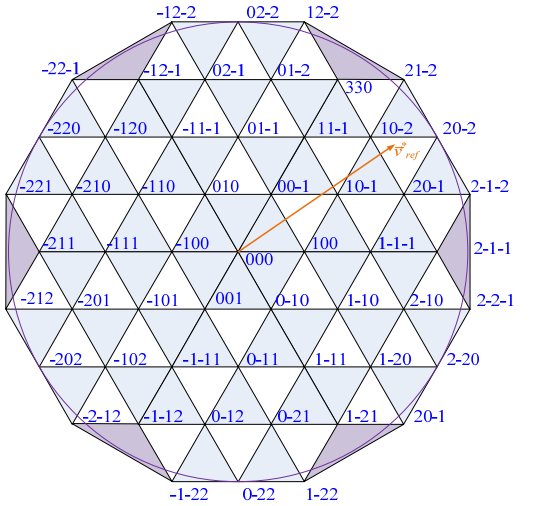

Fig. 3. Space vector diagram of the modified SVPWM for CMV reduction in a 5L-ANPC inverter.

distinct switching states producing five levels in the output voltage as listed in Table I, where "j" denotes the phase of A, B, or C; and "1" and "0" represent the ON and OFF states of the switches, respectively. In the 5L-ANPC inverter, two voltage levels of $-V_{dc}/4$ and $V_{dc}/4$ can be produced by two different switching states, referred to as redundant switching states, which affect the DC-link capacitor and flying capacitor voltages differently. For example, the voltage level of $V_{dc}/4$ can be produced by the switching states of V_5 and V_6. The redundant switching states of V_3 and V_4, with a voltage level of 0 V, are exploited to keep the fundamental operation of the higher-voltage-rated switches since they have the same effect on the capacitor voltages. It is noted that the switching states of S_{j1} and S_{j2}, which are always the same, and can be controlled by the same gating signal.

C. CMV of 5L-ANPC inverters

The CMV of a VSI is defined as the voltage difference between the neutral point of the load and the mid-point of the DC-link voltage as shown in Fig. 1(b). For a three-phase VSI, the CMV can be expressed as [6]:

$$v_{NO} = (v_{AO} + v_{BO} + v_{CO})/3 \quad (1)$$

TABLE II.

SELECTED SWITCHING STATES FOR CAPACITOR VOLTAGE CONTROL.

Flying capacitor voltage control signal	DC-link capacitor voltage control signal	Switching states
$Sig\_Fly_j > 0$	$Sig\_DC_j > 0$	V_0, $\boldsymbol{V_1}$, V_3, V_4, $\boldsymbol{V_5}$, V_7
$Sig\_Fly_j < 0$	$Sig\_DC_j < 0$	V_0, $\boldsymbol{V_2}$, V_3, V_4, $\boldsymbol{V_6}$, V_7

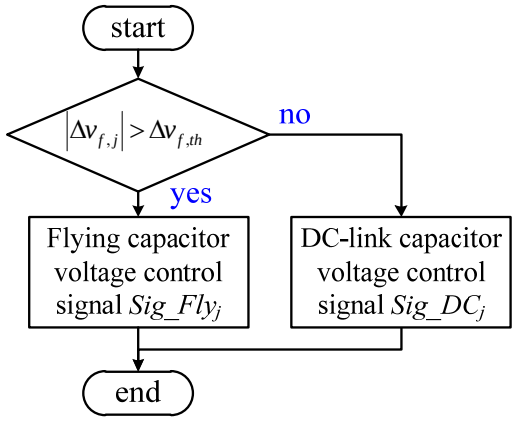

Fig. 4. Flowchart for choosing a voltage control signal.

where v_{AO}, v_{BO}, and v_{CO} are the pole voltages of the inverter.

A diagram of the SVPWM of a 5L-ANPC inverter is illustrated in Fig. 2, which includes 125 voltage vectors [23]. The CMV generated by these voltage vectors can be expressed as [7]:

$$v_{NO} = \frac{V_{dc}}{12}\left(S_A + S_B + S_C\right) \tag{2}$$

where S_A, S_B, and S_C are the switching function for each of the inverter legs. The CMV of a 5L-ANPC inverter with the conventional PWM was not mentioned in [22], [23], where the magnitude of the CMV can reach $V_{dc}/2$ in the worst case [7].

III. CMV REDUCTION TECHNIQUE IN 5L-ANPC INVERTERS

A. Selection of a Voltage Vector for Low CMVs

In this paper, the SVPWM for CMV reduction utilizes only 55 voltage vectors producing low CMV values, which involve $-V_{dc}/12$, *0* V, and $V_{dc}/12$, among the 125 voltage vectors of a three-phase 5L-ANPC inverter [17]. A space vector diagram of the modified SVPWM is shown in Fig. 3. It excludes the six voltage vectors located at the vertices of the hexagon, which have a high value for the CMV, ±Vdc/6. Then the DC-link voltage of the inverter can be utilized in the full range.

B. Control of Capacitor Voltages under Low CMV Conditions

The capacitor voltages of a 5L-ANPC inverter need to be controlled precisely. The flying capacitor voltages of each phase leg are regulated at $V_{dc}/4$. Thus, their deviation is expressed as:

$$\Delta v_{f,j} = v_{f,j} - V_{dc}/4 \tag{3}$$

where $v_{f,j}$ is the flying capacitor voltage of phase ***j***. Meanwhile, the DC-link capacitor voltages are controlled at $V_{dc}/2$. Therefore, the deviation of the neutral-point voltage (NPV) is expressed as:

$$\Delta v_n = \frac{v_{C2} - v_{C1}}{2} \tag{4}$$

where v_{C1} and v_{C2} are the voltages of the upper and lower DC-link capacitors, respectively.

At a pole voltage level of $-V_{dc}/4$, which is produced by the switching states of V_1 or V_2, the flying capacitor voltage is discharged with the switching states of V_1 when the positive current flows. Otherwise, the flying capacitor voltage is charged by the switching state of V_2. On the other hand, if the current is negative, the switching states of V_1 or V_2 charge or discharge the flying capacitor, respectively.

The control signal parameters Sig_Fly_j and Sig_DC_j of flying capacitor and DC-link capacitor voltages are used to select the redundant switching states of the capacitor voltage control. The control signal of the flying capacitor voltages is defined as:

$$Sig\_Fly_j = \Delta v_{f,j} i_j \tag{5}$$

where i_j is the current of phase ***j***. By the control signal of the flying capacitor voltage, appropriate redundant switching states of the 5L-ANPC inverter are selected and listed in Table II.

Considering the deviation of the NPV at the pole voltage level of $-V_{dc}/4$, the switching state of V_1 does not affect the NPV deviation. Meanwhile, the switching state of V_2 causes a decrease or increase in the deviation of the NPV when a positive or negative current flows, respectively. For this reason, the control signal of the DC-link capacitor voltage is defined as:

$$Sig\_DC_j = \Delta v_n i_j v_j^* \tag{6}$$

where i_j and v_j^* are the current and reference voltage of phase ***j***, respectively.

As listed in Table II, the corresponding redundant switching states are chosen for minimizing the NPV deviation. For example, negative values of Δv_n, i_j and v_j^* causes the Sig_DC_j to be negative. Thus, the deviation of the NPV is increased since the lower capacitor voltage, v_{C2}, is charged by the switching state of V_2. Meanwhile, a positive current causes Sig_DC_j to be positive with negative values of Δv_n and v_j^*. Then the switching state of V_1 is selected to avoid decreasing the deviation of the NPV further. In other words, the switching state of V_2 is not chosen since the switching state of V_2 can result in an undesirable decrease in the NPV deviation. In conclusion, the deviation of the NPV can be increased by the other two phase-legs to minimize the NPV deviation.

The influence of redundant switching states on the DC-link and flying capacitor voltages of a 5L-ANPC inverter with the control signal of the flying capacitor and DC-link capacitor voltages are illustrated in Fig. 4. When the magnitude of $\Delta v_{f,j}$ is lower than its constraint value, $\Delta v_{f,th}$, the control signal parameter of the DC-link capacitor voltage is chosen as shown in Fig. 4. Otherwise, the redundant switching

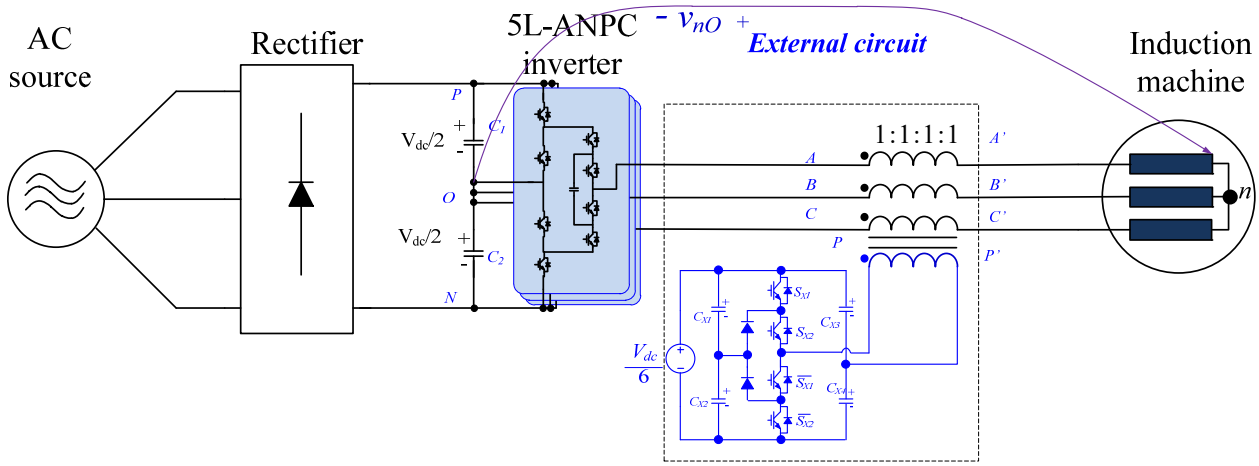

Fig. 5. Proposed auxiliary circuit for CMV elimination by a NPC leg.

states are chosen based on the control signal of the flying capacitor voltage, Sig_Fly_j.

As a result, for a 5L-ANPC inverter with the modified SVPWM, the CMV varies among the three voltage levels of $V_{dc}/12$, 0 V, and $V_{dc}/12$. In addition, the DC-link and flying capacitor voltages are regulated, and the maximum utilization of the DC-link voltage is kept at the unity modulation index (MI).

IV. Proposed CMV Elimination Method

A. Configuration of the Auxiliary Circuit

With the modified PWM, the CMV cannot be fully eliminated for a 5L-ANPC inverter. To achieve this goal, an additional circuit is needed. In this paper, an auxiliary circuit is suggested, which consists of an NPC leg and a CMT, as shown in Fig. 5. The four active switches of the NPC leg are connected in series and divided into two complementary pairs, which are S_{X1} and $\overline{S}_{X1}$; and S_{X2} and $\overline{S}_{X2}$. The active circuit is supplied by a low-power voltage-source of $V_{dc}/6$, where the neutral point is created by two capacitors connected in series. The CMT involves four windings, where the primary winding is supplied by the active circuit and the three secondary windings are inserted between the inverter output terminal and the load. It should be noted that only the magnetizing current flows on the primary side, which results in a small size of the primary winding.

B. Operating Principle of the Proposed Method

A NPC leg with a DC source of $V_{dc}/6$ can generate three voltage levels of $-V_{dc}/12$, 0 V, and $V_{dc}/12$, which are equal to those of the CMV in the 5L-ANPC inverter with the modified SVPWM. That is:

$$v_{PP'} = v_{AA'} = v_{BB'} = v_{CC'} = v_{CMV}. \quad (7)$$

With the auxiliary half-bridge circuit and the CMT, the CMV in (1) can be expressed as:

$$v_{CMV'} = \frac{v_{A'O} + v_{B'O} + v_{C'O}}{3} \quad (8)$$

which can be decomposed into two terms as:

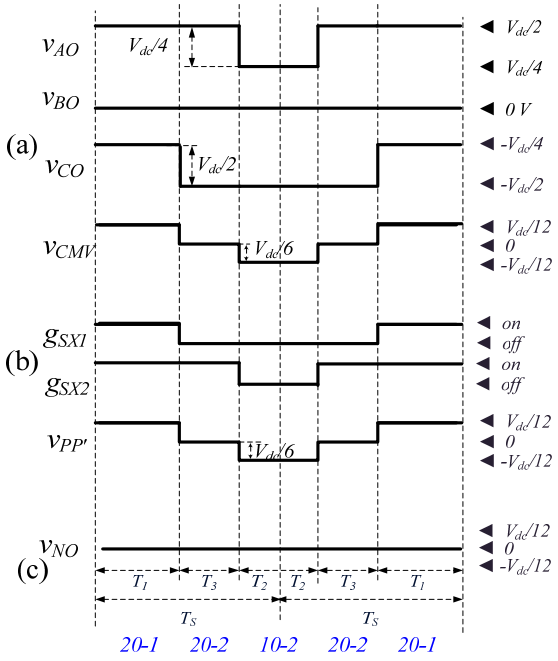

Fig. 6. Operating principle of the proposed method.

$$v_{CMV'} = \frac{v_{A'A} + v_{B'B} + v_{C'C}}{3} + \frac{v_{AO} + v_{BO} + v_{CO}}{3}. \quad (9)$$

Substituting (1) and (7) into (9) yields:

$$v_{CMV'} = -v_{CMV} + v_{CMV} = 0. \quad (10)$$

It should be noted that the CMV of the inverter is effectively cancelled by the auxiliary circuit. Depending on the voltage vectors of the SVPWM, the gating signals of the NPC leg are controlled to compensate the CMV. For a CMV of $V_{dc}/12$, the switches S_{X1} and S_{X2} are turned ON. Meanwhile, S_{X1} is turned OFF and S_{X2} is turned ON during the interval of the voltage vectors with zero CMV. Otherwise, for the voltage vectors with a CMV of $-V_{dc}/12$, the switches S_{X1} and S_{X2} are turned OFF. The gating signal of the NPC leg is regulated at the same time as that of the SVPWM of the 5L-ANPC inverter.

The operating principle of the proposed scheme is shown in Fig. 6, while the reference voltage vector is located in the

TABLE III.

SIMULATION PARAMETERS OF 5L-ANPC INVERTERS.

Parameters	Value
DC-link voltage	4,600 V
DC-link capacitance	3,300 μF
Flying capacitance	1,650 μF
Switching frequency	2,000 Hz
Auxiliary capacitance (C_X)	470 μF
Rated output voltage	3,000 V
Rated output frequency	60 Hz
Rated load power	1,000 kW
Load power factor	0.98
Δv_{f_th}	41 V

SVPWM diagram shown in Fig. 3. The three pole-voltages and CMV without compensation of a 5L-ANPC inverter are shown in Fig. 6(a), in which the CMV is the average value of the three pole-voltages. The gating signals of the NPC leg and the compensatory voltage generated by NPC leg are illustrated in Fig. 6(b). For a voltage vector {20-1} with a CMV of $V_{dc}/12$, the gating signals of both g_{SX1} and g_{SX2} are turned ON during T_1. Thus, a compensating voltage of $V_{dc}/12$ is produced. For zero CMV of the voltage vector {20-2}, the gating signals of g_{SX1} and g_{SX2} are OFF and ON, respectively. Therefore, the zero compensating voltage is produced during T_3. For the other dwell time of the current sampling time interval, T_2, the voltage vector {10-2} is active for a CMV of $-V_{dc}/12$. Therefore, the gating signals of both g_{SX1} and g_{SX2} are OFF for the compensating voltage of $-V_{dc}/12$. Due to this requirement of the gating signals, g_{X1} and g_{X2}, of the half-bridge circuit, the dwell times of g_{X1} and g_{X2} can be obtained from T_1, T_2 and T_3 for the modified SVPWM of a 5L-ANPC inverter. Hence, the compensating voltage of the auxiliary half-bridge circuit is applied to the primary side of the CMT, which is the same as the CMV in terms of magnitude and phase.

Due to the half-bridge structure of the auxiliary circuit, the voltage supplying the primary winding has no DC component. If the output voltage of the auxiliary circuit contains a DC component, the voltage at the middle point of C_{X3} and C_{X4} varies to prevent the DC current. Therefore, the DC offset voltage is eliminated. As a result, the saturation of the CMT is avoided.

V. SIMULATION RESULTS

The effectiveness of the proposed scheme is verified by simulation results for a medium-voltage 5L-ANPC inverter. The parameters of the 5L-ANPC inverter and the auxiliary NPC leg for the simulation study are listed in Table III.

Simulation waveforms for the operating principles of the proposed method are shown in Fig. 7 for four switching cycles. The CMV of the inverter with the modified SVPWM for the CMV reduction varies among three voltage levels of –383 V, 0 V, and 383 V, which correspond with $-V_{dc}/12$, 0 V, and $V_{dc}/12$, as shown in Fig. 7(a). Then Fig. 7(b) shows the gating signals of the auxiliary NPC leg, where control is based on the value of the remaining CMV of the inverter as previously mentioned. g_{SX1} is ON only during the positive

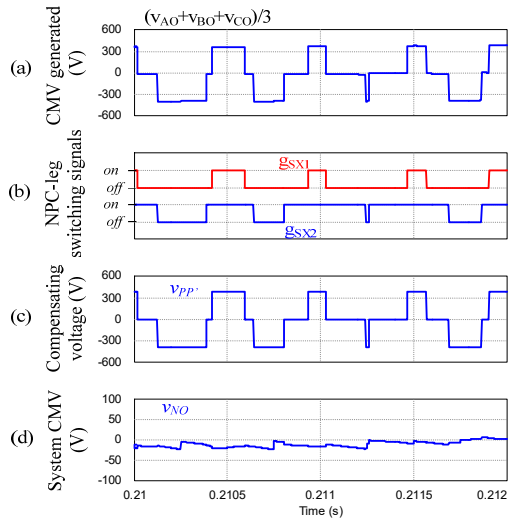

Fig. 7. Key waveforms for the CMV compensation: (a) CMV generated by a 5L-ANPC inverter with the reduction CMV method; (b) NPC leg switching signals; (c) compensating voltage produced by the NPC leg; (d) CMV of the load.

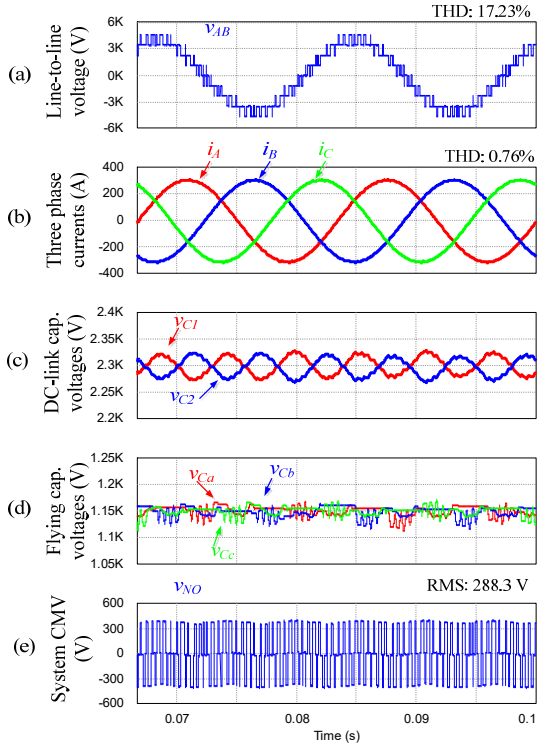

Fig. 8. Output performance of a 5L-ANPC inverter with the modified SVPWM for CMV reduction at the rated output voltage: (a) line-to-line voltage; (b) three phase currents; (c) DC-link capacitor voltages; (d) flying capacitor voltages; (e) CMV of the load.

CMV, $V_{dc}/12$, whereas g_{SX2} is OFF only during the negative CMV, $-V_{dc}/12$. Therefore, the compensating voltage of the NPC leg, as shown in Fig. 7(c), is applied to the primary winding of the CMT. Since the compensating voltage is identical to the CMV of the inverter in terms of magnitude and phase, the CMV of the load can be eliminated, as shown in Fig. 7(d). Due to fluctuations of the DC-link capacitor and flying capacitor voltages, the CMV of the inverter has a low

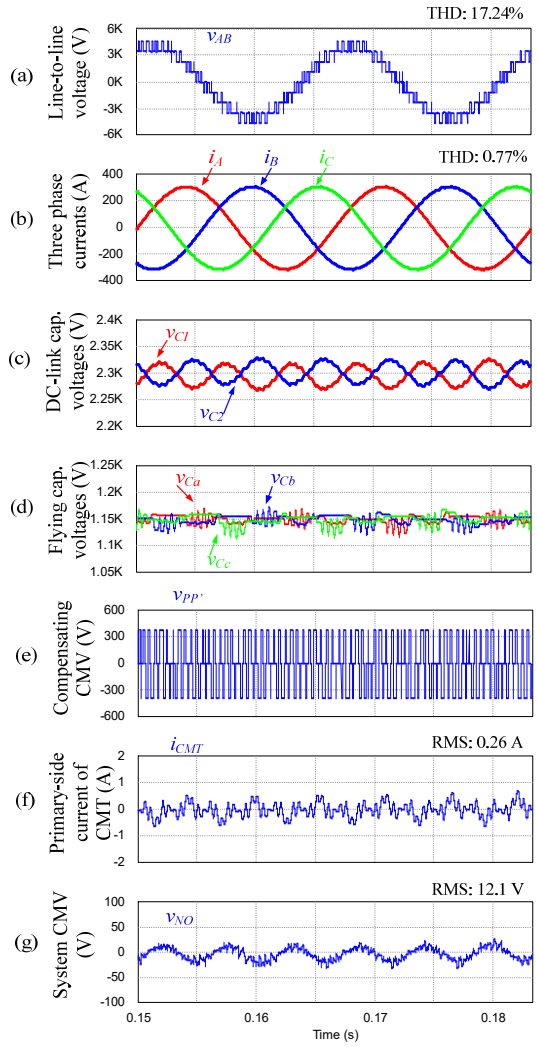

Fig. 9. Output performance of a 5L-ANPC inverter with the proposed scheme at the rated output voltage: (a) line-to-line voltage; (b) three-phase currents; (c) DC-link capacitor voltages; (d) flying capacitor voltages; (e) output voltage of the auxiliary leg; (f) primary-side current of the CMT; (g) CMV of the load.

value of variation.

The performance of a 5L-ANPC inverter with the modified SVPWM utilizing 55 voltage vectors is illustrated in Fig. 8 [17]. The line-to-line voltage, v_{AB}, has nine voltage steps with an approximately sinusoidal waveform, as shown in Fig. 8(a). The voltage THD, which is relatively low, is only 17.23%. Fig. 8(b) shows the three-phase currents with a low THD of 0.76%, which are balanced and sinusoidal. The DC-link capacitor voltages of the 5L-ANPC inverter are well balanced at a reference value of $V_{dc}/2$ with a peak ripple of about 1.1 %, as shown in Fig. 8(c). Fig. 8(d) shows the flying capacitor voltages of the inverter, which are regulated at a voltage level of $V_{dc}/4$ with a peak ripple of about 3 %. Then the CMV of the inverter is illustrated in Fig. 8(e), where its RMS and peak values are 288.3 V and 383.3 V, respectively.

The performance of a 5L-ANPC inverter with the proposed method is shown in Fig. 9. The line-to-line voltage and currents of the inverter are shown in Fig. 9(a) and (b), which are similar to those of Fig. 8(a) and (b), respectively.

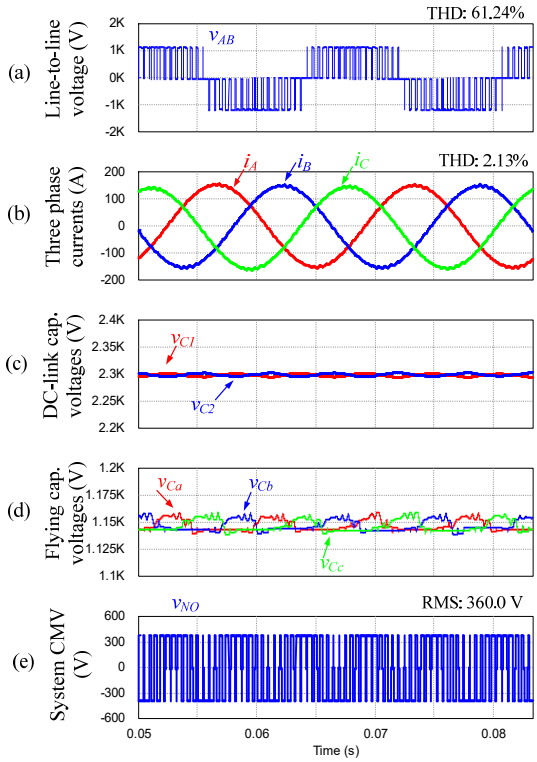

Fig. 10. Output performance of a 5L-ANPC inverter with the modified SVPWM for CMV reduction at a low MI (0.2) and a low power factor (PF=0.15): (a) line-to-line voltage; (b) three phase currents; (c) DC-link capacitor voltages; (d) flying capacitor voltages; (e) CMV of the load.

The DC-link and flying capacitor voltages of the inverter are well controlled at $V_{dc}/2$ and $V_{dc}/4$, respectively. Both the peak ripples of the DC-link and flying capacitor voltages with the proposed scheme are similar to those of Fig. 8. Due to the modulation, the compensating voltage of the auxiliary leg, as shown in Fig. 9(e), matches the CMV of the inverter, which varies among the three voltage levels of – 383.3 V, 0 V, and 383.3 V. Since the three phase currents of the inverter are balanced, only the magnetizing current flows on the primary winding of the CMT, where value is low, as shown in Fig. 9(f). Due to the proposed scheme, the CMV of the load is decreased to 12.1 V and 18 V in terms of the RMS and peak values, respectively, as shown in Fig. 9(g).

Fig. 10 shows the operating performance of an inverter with the CMV-reduction SVPWM [17] at a low MI and a low power factor. The line-to-line voltage is illustrated in Fig. 10(a) with three voltage levels and a high THD as in the two-level inverters. The three phase currents are also sinusoidal and balanced, as shown in Fig. 10(b). The DC-link and flying capacitor voltages, as shown in Fig. 10(c) and (d), are well regulated at their references with peak errors of 0.4 % and 1.3 %, respectively. The CMV of the inverter is kept at the three voltage levels of –383.3 V, 0 V, and 383.3 V, as shown in Fig. 10(e), where the RMS value of the CMV is 360 V.

The proposed scheme applied to an inverter operating at a low MI and a low power factor is shown in Fig. 11, which corresponds to Fig. 10. The line-to-line voltage, three phase-currents, DC-link capacitor voltages, and flying capacitor

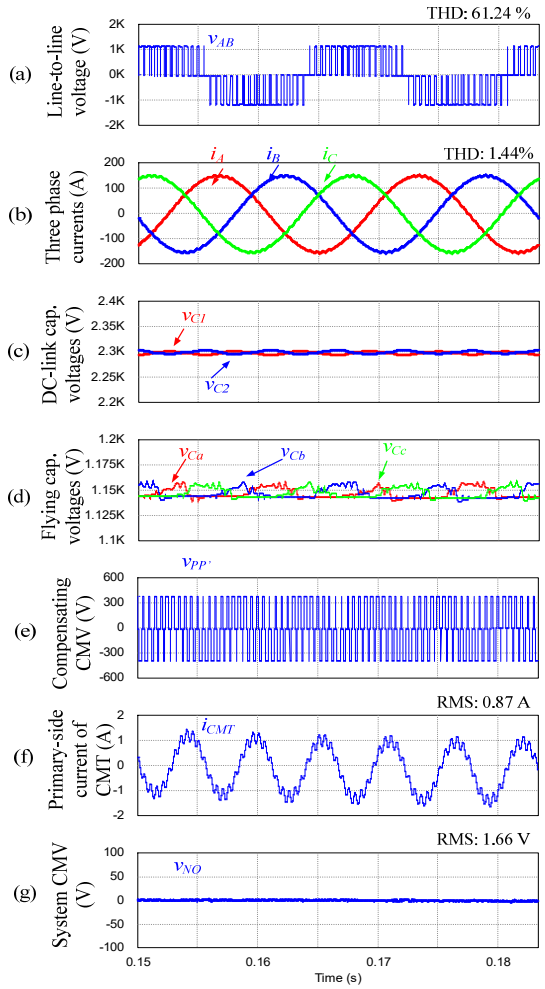

Fig. 11. Output performance of a 5L-ANPC inverter with the proposed scheme at a low MI (0.2) and a low power factor (PF=0.15): (a) line-to-line voltage; (b) three-phase currents; (c) DC-link capacitor voltages; (d) flying capacitor voltages; (e) output voltage of the auxiliary leg; (f) primary-side current of the CMT; (g) CMV of the load.

voltages, as shown in Fig. 11(a), (b), (c) and (d), are similar to those of Fig. 10(a), (b), (c) and (d), respectively. The compensating voltage for the CMV, as shown in Fig. 11(e), which is injected into the inverter system through the CMT, causes the cancellation of the CMV on the load side, as shown in Fig. 11(g). The primary current of the CMT is a low value of 0.87 A in RMS, as shown in Fig. 11(f).

VI. Experimental Results

The proposed scheme for CMV elimination has been tested for an experimental setup of a 5L-ANPC inverter with an additional NPC leg in the laboratory, where the prototype system is shown in Fig. 14. The parameters of the system are listed in Table IV. The IGBTs (SKM75GB12T4) of the inverter and the additional leg are controlled by a DSP chip (TMS320F28335). The 5L-ANPC inverter with the NPC leg is controlled by 22 PWM gating signals, which have been implemented by a Xilinx FPGA device (XC3S400-PQG208EGQ1321). The switching frequency of the inverter is 2,000 Hz.

Fig. 12(a) and (b) show the line-to-line voltage and three

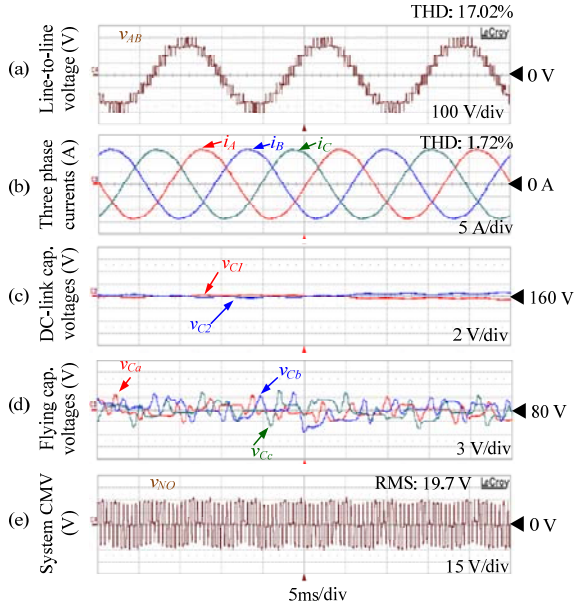

Fig. 12. Output performance of a 5L-ANPC inverter with the modified SVPWM for CMV reduction: (a) line-to-line voltage; (b) three phase currents; (c) DC-link capacitor voltages; (d) flying capacitor voltages; (e) CMV of the load.

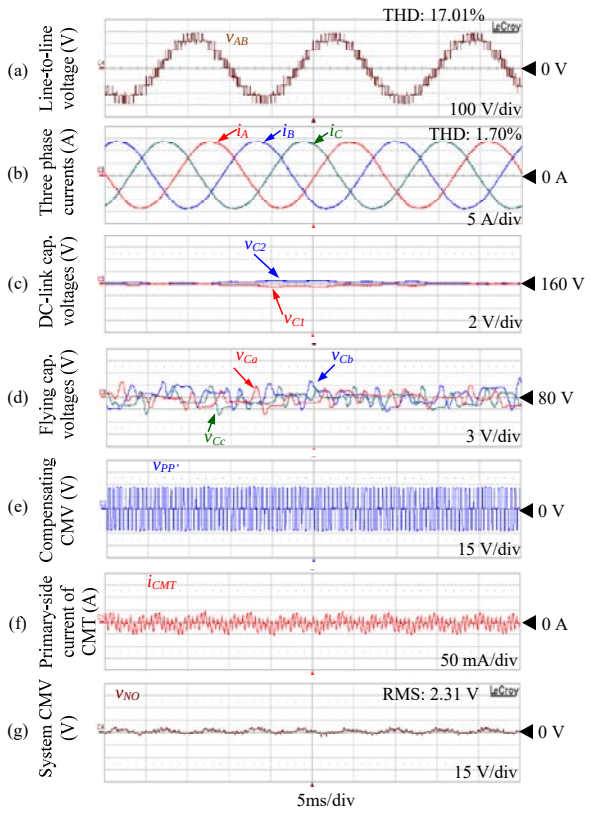

Fig. 13. Output performance of a 5L-ANPC inverter with the proposed scheme: (a) line-to-line voltage; (b) three-phase currents; (c) DC-link capacitor voltages; (d) flying capacitor voltages; (e) output voltage of the auxiliary leg; (f) primary-side current of the CMT; (g) CMV of the load.

phase currents of a 5L-ANPC inverter with the CMV-reduction SVPWM, respectively [17]. The line-to-line voltage waveform with a THD of 17.86 % has nine voltage levels. The three phase currents are balanced and sinusoidal with a low THD of 1.03%. The DC-link capacitor and flying capacitor voltages are well controlled, as shown in Fig. 12(c)

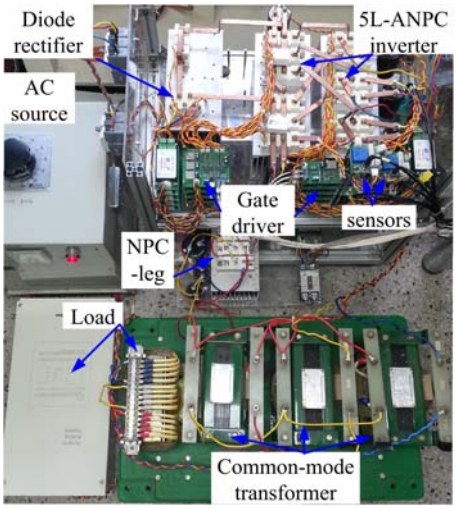

Fig. 14. Experimental setup.

TABLE IV.
PARAMETERS OF A 5L-ANPC INVERTER (EXPERIMENTAL).

Parameters		Value
DC-link voltage		320 V
DC-link capacitance		2,200 μF
Flying capacitance		1,000 μF
Switching frequency		2,000 Hz
Auxiliary capacitance (C_X)		470 μF
Rated output voltage		200 V
Rated output frequency		60 Hz
Rated load power		3 kW
Load power factor		0.98
$\Delta v_{f\ th}$		2 V

and (d), respectively. The ripple of the DC-link capacitor voltage is relatively low at 0.6 %. Meanwhile, that of the flying capacitor voltages is about 5 %. The CMV of the inverter with the modified SVPWM is shown in Fig. 12(e), where the peak and RMS values are 26.7 V and 19.7 V, respectively.

The performances of a 5L-ANPC inverter system with the proposed scheme at its rated output voltage are shown in Fig. 13, which corresponds to those of Fig. 12. The line-to-line voltage, three phase currents, DC-link capacitor voltages, and flying capacitor voltages, which are shown in Fig. 13(a) - (d), match those of Fig. 12. It should be noted that the output performance of the inverter is not changed. The compensating voltage generated by the NPC leg is shown in Fig. 13(e), which varies among the three voltage levels of –26.7 V, 0 V, and 26.7 V. The primary current of the CMT is shown in Fig. 13(f), which is a low value. The CMV at the load is shown in Fig. 13(g), which is low at 5 V_{peak}, and 2.31 V_{rms}. CMV still exists due to fluctuations of the DC-link capacitor and flying capacitor voltages and the parasitic inductance and capacitance of the system.

Test results for the modified SVPWM are shown in Fig. 15, at a low MI and a low fundamental frequency. The line-to-line voltage waveform has three voltage levels, as shown in Fig. 15(a). The three phase currents are shown in Fig. 15(b), which are sinusoidal and balanced. The DC-link and flying capacitor voltages are well regulated at $V_{dc}/2$ and $V_{dc}/4$, as

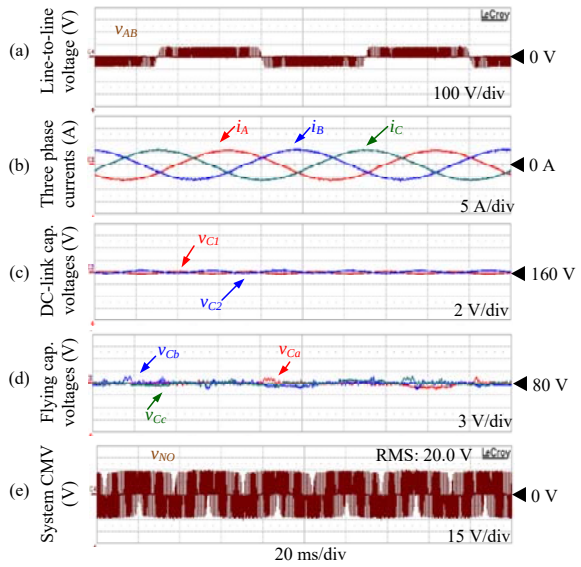

Fig. 15. Output performance of a 5L-ANPC inverter with the modified SVPWM for CMV reduction at a low MI (MI=0.2) and a low fundamental frequency (f=10 Hz): (a) line-to-line voltage; (b) three phase currents; (c) DC-link capacitor voltages; (d) flying capacitor voltages; (e) CMV of the load.

shown in Fig. 15(c) and (d), respectively. Due to the lower value of the load current, the ripples of the DC-link capacitor and flying capacitor voltages are reduced, which are 0.3 % and 1.9 %, respectively. The CMV of the inverter varies among the three voltage levels of $-V_{dc}/12$, 0 V, and $V_{dc}/12$, and its RMS value is 20.0 V, as shown in Fig. 15(e).

오류! 참조 원본을 찾을 수 없습니다.(a)-(d) show the line-to-line voltage, three phase currents, DC-link capacitor voltages, and flying capacitor voltages, which are similar to those of Fig. 15(a)-(d). The NPC leg produces a compensating voltage with three levels of –26.7 V, 0 V, and 26.7 V, as shown in **오류! 참조 원본을 찾을 수 없습니다.**(e), which is identical to the CMV of the inverter shown in Fig. 15(e). The primary current is still low since only the magnetizing current of the CMT flows. With the proposed scheme, the CMV of the inverter is almost eliminated at 1.79 V_{rms}, as shown in **오류! 참조 원본을 찾을 수 없습니다.**(g), where the CMV slightly exists due to fluctuations of the DC-link and flying capacitor voltages as well as the parasitic elements of the system.

VII. CONCLUSION

In this paper, a CMV elimination scheme for 5L-ANPC inverters has been the proposed, which utilizes both the CMV-reduction SVPWM, the auxiliary circuit of an NPC leg and a CMT. In the proposed method, the DC-link voltage utilization is not decreased and the switching frequency of the inverter is not increased. With the half-bridge NPC leg, saturation of the CMT can be avoided. The validity of the proposed method has been verified by simulation and experimental results.

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