Improved Control Strategy for T-type Isolated DC/DC Converters

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Abstract

T-type isolated DC/DC converters have recently attracted attention due to their numerous advantages, including few components, low cost, and symmetrical operation of transformers. This study proposes an improved control strategy for increasing the efficiency of T-type isolated DC/DC converters. Under the proposed strategy, the primary circulating current flows through the auxiliary switches (metal–oxide–semiconductor field-effect transistors) instead of their body diodes in free-wheeling periods. Such feature can reduce conduction losses, thereby improving the efficiency of T-type isolated DC/DC converters. The operation principles and performances of T-type isolated DC/DC converters under the proposed control strategy are analyzed in detail and verified through the simulation and experimental results.

Key words: DC/DC converter, T-type; Zero-voltage switching (ZVS).

I. INTRODUCTION

High-power isolated DC/DC converters with high efficiency and high reliability are widely studied in the field of modern power electronics because of their known advantages of galvanic isolation and high voltage conversion rate, which make them applicable to electric vehicles, telecommunications, solar systems, fuel cell systems, and DC transmission systems [1–7].

The most popular and useful topologies of isolated DC/DC converters are the two-level zero-voltage switching (ZVS) DC/DC converters, including half-bridge (HB) ZVS DC/DC converters and full-bridge ZVS DC/DC converters with phase-shift control [8–12], which feature high power density, easy control strategy, and simple circuit structure. The three-level (TL) ZVS isolated DC/DC converter was proposed for high input voltage applications because voltage stresses on the power switches are only half of the input voltage and voltage stress on the transformer can be reduced in comparison with two-level ZVS DC/DC converters. Therefore, low-voltage stress switches with small on-state resistance can improve the efficiency of TL ZVS DC/DC converters [13–22]. Numerous studies on TL DC/DC converters have focused on extending the soft switching range [16], [17], reducing the circulating currents [18], [19], balancing the two input voltages [20], [21], and reducing the ripple currents on the input capacitors [22].

T-type converters are another type of TL converter that can also produce three voltage levels, and thus, have become popular in single or three-phase inverters [23–26]. However, only a few studies have discussed T-type isolated DC/DC converters. In [27], a dual active bridge isolated DC/DC converter with a TL T-type leg and a corresponding modulation strategy were proposed. T-type isolated DC/DC converters with asymmetrical duty ratio control were proposed in [28] and [29] for high power and high efficiency applications. Compared with conventional diode-clamped TL isolated DC/DC converters, T-type isolated DC/DC converters feature fewer components and a simpler circuit structure. Table I shows the comparison results of the numbers of primary circuit components of HB T-type isolated DC/DC converters and conventional HB diode-clamped TL isolated DC/DC converters [13]. T-type converters are
derived from two-level converters, and thus, the main power switches in T-type converters must withstand input voltage. At present, conventional diode-clamped TL DC/DC converters are widely used in high input voltage applications [16–22] because their power switches are only required to withstand half of the input voltage. However, with the development of silicon carbide (SiC) power devices, TL T-type isolated DC/DC converters will be suitable for high input voltage applications because the drain–source breakdown voltage of SiC power devices is considerably higher than that of silicon (Si) power devices [30]. In addition, the isolation transformer of a T-type isolated DC/DC converter exhibits a symmetrical operation, which differs from that of an asymmetrical HB ZVS DC/DC converter whose transformer operates with DC current and flux offset [31].

**TABLE I**

<table>
<thead>
<tr>
<th>Component</th>
<th>HB diode-clamped TL isolated DC/DC converter</th>
<th>HB T-type isolated DC/DC converter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Switch</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>Clamping Diode</td>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>Flying Capacitor</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Input Capacitor</td>
<td>2</td>
<td>2</td>
</tr>
</tbody>
</table>

In the present work, an improved control strategy is proposed to improve the efficiency of T-type isolated DC/DC converters. In conventional control strategies, the primary current flows through the body diodes of switches. By contrast, the primary current under the proposed control strategy flows through auxiliary switches, i.e., metal–oxide–semiconductor field-effect transistors (MOSFETs), in free-wheeling periods. Therefore, the proposed control strategy can effectively boost the efficiency of converters. In addition, the proposed control strategy can achieve ZVS, which can reduce switching losses. The operation principles and performances of T-type isolated DC/DC converters under the proposed control strategy are analyzed in detail. The proposed control strategy is also verified through the simulation and experimental results.

The rest of this paper is organized as follows. Section II presents an analysis of the operation principles of the proposed control strategy in detail. Section III discusses the analysis of the characteristics and performances of T-type isolated DC/DC converters under the proposed control strategy. Section IV cites the simulation and experimental results to verify the proposed control strategy. Finally, Section V describes the main contributions of this work.

**II. OPERATION PRINCIPLES OF THE PROPOSED CONTROL STRATEGY**

Fig. 1 shows the circuit structure of a T-type isolated DC/DC converter. At the primary side, $C_1$ and $C_2$ are two input capacitors that split the input voltage $V_{in}$ into $V_1$ and $V_2$. $S_1$–$S_4$ are the power switches. $D_1$–$D_4$ are the diodes of $S_1$–$S_4$. $C_{1a}$–$C_{4a}$ are the parasitic capacitors of $S_1$–$S_4$. $T_r$ is the transformer. $L_o$ is the leakage inductor of the transformer $T_r$. At the secondary side, $D_{1a}$–$D_{4a}$ are four output rectifier diodes. $L_o$ and $C_o$ are the output filter inductor and capacitor, respectively. In Fig. 1, $V_{o1}$ is the input voltage; $V_{o2}$ is the voltage between points a and b; $i_p$ is the primary current of the transformer; $i_{o1}$ is the current flowing through the output filter inductor; $V_o$ and $i_o$ are the output voltage and current, respectively; and $n$ is the turns ratio of the transformer $T_r$. $i_{o1,s1}$, $i_{o2,s2}$, $i_{o3,s3}$, and $i_{o4,s4}$ are the currents flowing through $(S_1, D_1)$, $(S_2, D_2)$, $(S_3, D_3)$, and $(S_4, D_4)$, respectively. In the T-type isolated DC/DC converter, $S_1$ and $S_2$ are the main switches that withstand the input voltage, whereas $S_3$ and $S_4$ are the auxiliary switches that withstand only half of the input voltage. Hence, a low-voltage stress switch (MOSFET) can be used for $S_3$ and $S_4$ even in high-voltage applications.

Several assumptions are derived to simplify the theoretical analysis. 1) All the switches and diodes are ideal. 2) $S_1$ and $S_2$ have the same parasitic capacitor, and thus, $C_{1a} = C_{2a} = C_{12}$. $S_3$ and $S_4$ have the same parasitic capacitor, and thus, $C_{3a} = C_{4a} = C_{34}$. 3) The two input capacitors $C_1$ and $C_2$ are sufficiently large to be considered two voltage sources with the value of $V_{in}/2$. 4) The output filter inductor $L_o$ is sufficiently large to be considered a constant current source.

Fig. 2 shows the operation principles of a conventional control strategy [28] and the proposed control strategy. In this figure, $d_{s1}$–$d_{s4}$ are the driving signals of switches $S_1$–$S_4$; $d_1$ is the duty cycle of switches $S_1$ and $S_2$; $i_{S1}$, $i_{S2}$, $i_{S3}$, and $i_{S4}$ are the currents flowing through switches $S_1$–$S_4$; $i_{D1}$, $i_{D2}$, $i_{D3}$, and $i_{D4}$ are the currents flowing through diodes $D_1$–$D_4$; and $d_{loss}$ is the duty cycle loss in one switching period.

1) **Conventional control strategy**, as shown in Fig. 2(a): The duty ratios of auxiliary switches $S_3$ and $S_4$ are constant, and their values are both 0.5 if dead time is neglected. The output voltage $V_o$ is controlled by adjusting the duty ratios of the main switches $S_1$ and $S_2$ ($d_1$).

2) **Proposed control strategy**, as shown in Fig. 2(b): The driving signals of the switch pairs ($S_2$, $S_3$) and ($S_4$, $S_1$) are complementary. Therefore, time overlaps exist between the
driving signals of auxiliary switches $S_1$ and $S_4$, as highlighted in Fig. 2(b). The output voltage $V_o$ is also controlled by adjusting the duty ratios of main switches $S_1$ and $S_3$ ($d_1$).

The main difference between the two control strategies is the flow of currents through $S_3, S_4$ and $D_3, D_4$ ($i_{S3}, i_{S4}$ and $i_{D3}, i_{D4}$), as highlighted in Fig. 2. In the conventional control strategy, the primary current $i_p$ flows through the body diodes $D_3$ and $D_4$ in the free-wheeling periods, as highlighted in Fig. 2(a). Under the proposed control strategy, the primary current $i_p$ mainly flows through switches $S_3$ and $S_4$ instead of body diodes $D_3$ and $D_4$ in the free-wheeling periods, as highlighted in Fig. 2(b). In general, the power losses of the switch (MOSFET) are smaller than those of the body diode when the same currents flow through them [32]. Consequently, the proposed control strategy effectively reduces conduction losses and improves the efficiency of the converter compared with the conventional control strategy.

Fig. 2. Operation principles with main waveforms. (a) Conventional control strategy in [28]. (b) Proposed control strategy.

Fig. 3 shows the equivalent circuits to explain the operation principles of the T-type isolated DC/DC converter under the proposed control strategy shown in Fig. 2(b).

Stage 0 [before $t_0$]: During this period, switches $S_1$ and $S_3$ are at the on-state. Thus, voltage $V_{ab}$ is equal to $V_o/2$, and input power transfers to the load from $D_1$ and $D_4$. In this stage, the primary current $i_p$ is $i_o/n$.

Stage 1 [$t_0$–$t_1$]: Switch $S_1$ is turned off at $t_0$. Then, output current $i_o$ is reflected onto the primary side. In this case, the primary current $i_p$ remains $i_o/n$ to charge $C_{s1}$ and discharge $C_{s2}$ and $C_{s4}$. Therefore, the voltage of $C_{s1}$ ($V_{C_{s1}}$) increases, whereas the voltages of $C_{s2}$ ($V_{C_{s2}}$) and $C_{s4}$ ($V_{C_{s4}}$) decrease.

Stage 2 [$t_1$–$t_3$]: $V_{C_{s1}}$ increases to $V_o/2$ at $t_1$, and $V_{C_{s2}}$ and $V_{C_{s4}}$ decrease to $V_o/2$ and 0 V, respectively. Then, body diode $D_4$ conducts, thereby clamping $V_{C_{s4}}$ at 0 V. During this stage, $V_{ab}$ is maintained at 0 V, and $i_p$ remains $i_o/n$ and flows through $S_3, D_4, L_r$, and $T_r$. Therefore, the current on body diode $D_3$ ($i_{D3}$) is $i_o/n$.

Stage 3 [$t_2$–$t_3$]: Switch $S_4$ is turned on at zero voltage at $t_2$. Then, primary current $i_p$ starts to flow through $S_3, S_4, L_r$, and $T_r$. During this stage, primary current $i_p$ and voltage $V_{ab}$ remain $i_o/n$ and 0 V, respectively.

Stage 4 [$t_3$–$t_4$]: Switch $S_1$ is turned off at $t_3$. Then, the voltages of $C_{s1}$ ($V_{C_{s1}}$) and $C_{s3}$ ($V_{C_{s3}}$) increase, the voltage of
$C_{s2}$ ($V_{C2}$) decreases, and voltage $V_{ab}$ starts to decrease. Primary current $i_p$ starts to decrease and is insufficient to provide output current $i_o$. Thus, output rectifier diodes $D_{31}$, $D_{23}$, $D_{33}$, and $D_{44}$ conduct simultaneously, thereby clamping both the primary and secondary voltages of the transformer at 0 V. Therefore, voltage $V_{ab}$ is fully applied to $L_r$. During this stage, $L_r$ resonates with $C_{sn}$, $C_{s2}$, and $C_{s3}$.

Stage 5 [$t_4$–$t_5$]: $V_{C1}$ and $V_{C3}$ increase to $V_{in}$ and $V_{ab}/2$, respectively, at $t_4$; and $V_{C2}$ decreases to 0 V. Then, body diode $D_2$ begins to conduct, thereby clamping $V_{C2}$ at 0 V. Voltage $V_{ab}$ decreases to $-V_{ab}/2$. During this stage, 1) the primary current $i_p$ flows through $C_{s2}$, $D_2$, $L_r$, and $T_r$, in which case the current on the body diode $D_2$ ($i_{b2}$) is equal to $i_p$. In addition, 2) output rectifier diodes $D_{21}$, $D_{23}$, $D_{33}$, and $D_{44}$ continue to conduct, and thus, the voltage on $L_r$ is $-V_{ab}/2$, and $i_p$ decreases linearly.

Fig. 3. Equivalent circuits under the proposed control strategy. (a) [before $t_6$]. (b) [$t_6$–$t_1$]. (c) [$t_1$–$t_2$]. (d) [$t_2$–$t_3$]. (e) [$t_3$–$t_4$]. (f) [$t_4$–$t_5$]. (g) [$t_5$–$t_6$]. (h) [$t_6$–$t_7$]. (i) [$t_7$–$t_8$].
Stage 6 \([t_5-t_6]\): Switch \(S_2\) is turned on at zero voltage at \(t_5\), and primary current \(i_p\) goes through \(C_2, S_2, L_n\), and \(T_r\). During this stage, primary current \(i_p\) continues to decrease linearly.

Stage 7 \([t_6-t_7]\): Primary current \(i_p\) decreases to 0 A at \(t_6\) which indicates that the current direction of \(i_p\) changes. The voltage on \(L_r\) remains \(-V_{in}/2\). Therefore, \(i_p\) still decreases linearly.

Stage 8 \([t_7-t_8]\): Primary current \(i_p\) decreases at \(t_7\) to the negative reflected output current whose value is \(-i/n\). Then, \(D_3\) and \(D_4\) are turned off, and input power begins to transfer to the load from \(D_{12}\) and \(D_{33}\).

Switch \(S_2\) is turned off at \(t_8\). The second half cycle \([t_6-t_10]\) starts. The following analysis is similar to that of the first half cycle \([t_5-t_8]\), which is not repeated in this section.

### III. Characteristic Analysis of the Proposed Control Strategy

#### A. Voltage Stresses of Switches

In the T-type isolated DC/DC converter under the proposed control strategy, main switches \(S_1\) and \(S_2\) withstand the full input voltage \((V_{in})\), but auxiliary switches \(S_3\) and \(S_4\) are only required to withstand half of the input voltage \((V_{in}/2)\). Hence, the low-voltage stress switch (MOSFET) can be selected for auxiliary switches \(S_3\) and \(S_4\).

#### B. Duty Cycle Loss

In Fig. 2(b), the periods \([t_5-t_6]\) and \([t_{11}-t_{13}]\) are the times of the duty cycle losses in one switching period. In general, the periods \([t_5-t_6]\) and \([t_{11}t_{12}]\) are sufficiently short to be neglected; thus, \([t_5-t_6]\) and \([t_{11}-t_{13}]\) can be calculated by

\[
t_5 - t_6 = t_{13} - t_{11} = \frac{4 \cdot L_r \cdot i_t}{n \cdot V_{in}}.
\]

In accordance with (1), the duty cycle loss \(d_{loss}\) shown in Fig. 2(b) can be obtained as

\[
d_{loss} = \frac{t_5 - t_6}{T_r} = \frac{t_{13} - t_{11}}{T_r} = \frac{4 \cdot L_r \cdot i_t}{n \cdot V_{in} \cdot T_r}.
\]

#### C. Output Characteristic

When duty cycle loss is considered, the average output voltage \(V_o\) can be calculated by

\[
V_o = \frac{V_{in}}{n} \cdot (d_t - d_{loss}) = \frac{V_{in}}{n} \cdot (d_t - \frac{4 \cdot L_r \cdot i_t}{n \cdot V_{in} \cdot T_r}).
\]

In accordance with (3), the duty ratio \(d_t\) shown in Fig. 2 can be expressed by

\[
d_t = \frac{V_{in} \cdot n + 4 \cdot L_r \cdot i_t}{n \cdot V_{in} \cdot T_r}.
\]

#### D. Currents through Switches and Body Diodes

1) Conventional Control Strategy

In the conventional control strategy shown in Fig. 2(a), the root mean square (RMS) values of the currents through switches \(S_1\) and \(S_4\), namely, \(i_{33 \_rms\_con}\) and \(i_{44 \_rms\_con}\) can be given by

\[
i_{33 \_rms\_con} = i_{44 \_rms\_con} = \frac{i}{n} \cdot \sqrt{(0.5 - d_t)}.
\]

When (4) is substituted into (5), (5) can be rewritten as

\[
i_{33 \_rms\_con} = i_{44 \_rms\_con} = \frac{i}{n} \cdot \sqrt{0.5 - \frac{4 \cdot L_r \cdot i_t}{n \cdot V_{in} \cdot T_r}}.
\]

In practical operations, the periods \([t_5-t_6]\) and \([t_7-t_8]\) shown in Fig. 2(a) are significantly short. If these periods are neglected, then the average values of the currents flowing through body diodes \(D_3\) and \(D_4\), namely, \(i_{3 \_avg\_con}\) and \(i_{4 \_avg\_con}\) can be given by

\[
i_{3 \_avg\_con} = i_{4 \_avg\_con} = \frac{i}{n} \cdot \sqrt{0.5 - d_t}.
\]

When (4) is substituted into (7), (7) can be rewritten as

\[
i_{3 \_avg\_con} = i_{4 \_avg\_con} = \frac{i}{n} \cdot \sqrt{0.5 - \frac{4 \cdot L_r \cdot i_t}{n \cdot V_{in} \cdot T_r}}.
\]

2) Proposed Control Strategy

In the proposed control strategy shown in Fig. 2(b), the periods \([t_5-t_6]\) and \([t_6-t_{10}]\) are dead times and typically short. If these dead times are neglected, then the RMS values of the currents flowing through switches \(S_1\) and \(S_4\), namely, \(i_{33 \_rms\_pro}\) and \(i_{44 \_rms\_pro}\) can be given by

\[
i_{33 \_rms\_pro} = i_{44 \_rms\_pro} = \frac{i}{n} \cdot \sqrt{(1 - 0.5 - d_t)}.
\]

When (4) is substituted into (9), (9) can be rewritten as

\[
i_{33 \_rms\_pro} = i_{44 \_rms\_pro} = \frac{i}{n} \cdot (1 - \frac{2 \cdot V_{in} \cdot n \cdot i_t}{Y_{in} \cdot T_r} - \frac{8 \cdot L_r \cdot i_t}{n \cdot V_{in} \cdot T_r}).
\]

The dead times \([t_5-t_6]\) and \([t_6-t_{10}]\) are typically short in practical operations; hence, the average values of the currents flowing through body diodes \(D_3\) and \(D_4\) are extremely small, as shown in Fig. 2(b). Therefore, in the proposed control strategy, the circulating currents mainly flow through switches \(S_3\) and \(S_4\) instead of body diodes \(D_3\) and \(D_4\) in free-wheeling periods.

From (5)-(10) and the circuit parameters of the experimental prototype in the Appendix, the theoretical calculation results for the total power losses of switches \(S_3\) and \(S_4\) and their body diodes \(D_3\) and \(D_4\) (MOSFETs) [33] are presented in Fig. 4, which also shows the results with various output powers, including 500 W, 750 W, and 1 kW. As shown in Fig. 4, the total power losses of switches \(S_3\) and \(S_4\) and their body diodes \(D_3\) and \(D_4\) (MOSFETs) under the proposed control strategy are considerably lower than those under the conventional control strategy.
E. ZVS Achievement Conditions

1) Main Switches \( S_1 \) and \( S_2 \)

The energy stored in the leakage inductance (and the resonant inductor, if added to the circuit) is used to achieve the zero-voltage switch-on for main switches \( S_1 \) and \( S_2 \). Then, (11) should be satisfied to achieve the zero-voltage switch-on of switches \( S_1 \) and \( S_2 \).

\[
\frac{1}{2} L \left( \frac{1}{n} \right)^2 \geq \frac{1}{2} C_{s1} \cdot \left( \frac{V}{2} \right)^2 + \frac{1}{2} C_{s2} \cdot \left( \frac{V}{2} \right)^2 + \frac{1}{2} C_{s4} \cdot \left( \frac{V}{2} \right)^2
\]

\[
= \frac{1}{2} C_{s1} \cdot V_n^2 + \frac{1}{8} C_{s2} \cdot V_n^2
\]

(11)

In accordance with (11), the leakage inductance \( L_r \) should satisfy (12) to realize the zero-voltage switch-on of main switches \( S_1 \) and \( S_2 \) under a certain output power.

\[
L_r \geq \frac{n^2 \cdot V_n^2 \cdot (4 \cdot C_{s1} + C_{s2})}{4 \cdot I_n^2} \quad (12)
\]

2) Auxiliary Switches \( S_3 \) and \( S_4 \)

The zero-voltage switch-on of auxiliary switches \( S_3 \) and \( S_4 \) are mainly determined by the reflected current from the output filter inductor. In general, the output filter inductance is sufficiently large to enable switches \( S_3 \) and \( S_4 \) to achieve zero-voltage switch-on even at a light load. For example, energy \( E_1 \) is required to discharge parasitic capacitors \( C_{s2} \) and \( C_{s4} \) and charge parasitic capacitor \( C_{s1} \) to ensure the zero-voltage switch-on of switch \( S_4 \). The expression is as follows:

\[
E_1 \geq \frac{1}{2} C_{s1} \cdot \left( \frac{V}{2} \right)^2 + \frac{1}{2} C_{s2} \cdot \left( \frac{V}{2} \right)^2 + \frac{1}{2} C_{s4} \cdot \left( \frac{V}{2} \right)^2
\]

\[
= \frac{1}{2} C_{s1} \cdot V_n^2 + \frac{1}{8} C_{s2} \cdot V_n^2
\]

(13)

IV. SIMULATION AND EXPERIMENTAL VERIFICATION

A. Simulation Verification

A simulation model is built in PLECS \(^\circledR\) to verify the proposed control strategy. The model parameters are listed in the Appendix. In the simulation, the input voltage \( V_{in} \) is 400 V, the output voltage \( V_o \) is 50 V, and the output power \( P_o \) is 500 W. Figs. 5(a) and 5(b) show the simulation results under the conventional control strategy in [28] and the proposed control strategy, respectively. In the figures, \( i_{ds,S1} \) and \( i_{ds,S2} \) are the currents flowing through \( (S_1, D_1) \) and \( (S_2, D_2) \), \( i_{s3} \) and \( i_{s4} \) are the currents flowing through switches \( S_3 \) and \( S_4 \), and \( i_{d3} \) and \( i_{d4} \) are the currents flowing through body diodes \( D_3 \) and \( D_4 \) of \( S_3 \) and \( S_4 \).

As shown in the highlighted areas in Fig. 5(a), primary current \( i_p \) flows through body diodes \( D_1 \) and \( D_4 \) in the free-wheeling periods under the conventional control strategy.
By contrast, under the proposed control strategy, primary current $i_p$ goes through switches $S_3$ and $S_4$ in the free-wheeling periods, as shown in the highlighted areas in Fig. 5(b). Such characteristic can effectively reduce conduction losses and improve the efficiency of converters.

B. Experimental Verification

A 1 kW experimental prototype is established to verify the proposed control strategy. The circuit parameters of the prototype are listed in the Appendix. Fig. 6 shows the hardware of the established experimental prototype, which is controlled by dSPACE in the experiments. In the following experiments, a single PI control loop is designed to control the output voltage $V_o$ by adjusting the duty ratio $d_1$ shown in Fig. 2.

![Fig. 6. Hardware of the established experimental prototype.](image)

Fig. 7 shows the experimental results, including $V_{in}, V_o, V_{ab},$ and $i_p$, under the proposed control strategy when the output power $P_o$ is 1 kW, the input voltage $V_{in}$ is 400 V, and the output voltage $V_o$ is 50 V.

![Fig. 7. Experimental results, including $V_{in}, V_o, V_{ab},$ and $i_p$, under the proposed control strategy when $V_{in} = 400$ V, $V_o = 50$ V, and $P_o = 1$ kW.](image)

Figs. 8 and 9 show the comparison between the conventional control strategy in [28] and the proposed control strategy. In this work, $i_{ds,S3}$ and $i_{ds,S4}$ are the currents of $(S_3, D_3)$ and $(S_4, D_4)$, respectively. $i_{ds,S3}$ and $i_{ds,S4}$ are highly similar, and thus, only $i_{ds,S4}$ is presented in this paper for explanation. Figs. 8 and 9 indicate the following. 1) The values of $i_{ds,S2}$ are the same in the two control strategies. 2) Under the conventional control strategy, $i_{ds,S4}$ flows through body diode $D_4$ in the free-wheeling periods, as highlighted in Figs. 7(a) and 8(a), because $S_4$ is turned off. 3) Under the proposed control strategy, $i_{ds,S4}$ flows through switch $S_4$ in the free-wheeling periods, as highlighted in Figs. 7(b) and 8(b), because $S_4$ is turned on. The analysis in 2) and 3) indicates that the efficiency of converters improves more evidently under the proposed control strategy than under the conventional control strategy because the power loss of the switch is smaller than that of its body diode when the same currents flow through them.
Fig. 9. Experimental results when $V_{in} = 400$ V, $V_o = 50$ V, and $P_o = 1$ kW. (a) Conventional control strategy in [28]. (b) Proposed control strategy.

Figs. 10–11 show the achieved ZVS conditions of the T-type isolated DC/DC converter under the proposed control strategy. Fig. 10 shows the primary current $i_{p}$, primary voltage $V_{ab}$, driving signal $V_{gsS_1}$, and drain–source voltage $V_{dsS_1}$ of the main power switch $S_1$, which realizes ZVS at 500 W and 1 kW.

In Fig. 10, the energy from the leakage inductance of the transformer is provided for main switch $S_1$ to achieve the zero-voltage switch-on. Fig. 11 shows the primary current $i_{p}$, primary voltage $V_{ab}$, driving signal $V_{gsS_3}$, and drain–source voltage $V_{dsS_3}$ of auxiliary power switch $S_3$, which realizes ZVS at 500 W and 1 kW. In Fig. 11, the energy from both the output filter inductance and leakage inductance of the transformer is provided for auxiliary switch $S_3$ to achieve zero-voltage switch-on. The achieved ZVS conditions of switches $S_2$ and $S_4$ are similar to those of switches $S_1$ and $S_3$, respectively, which are not repeated in this paper.

Fig. 12 shows the achieved ZVS conditions for switch $S_1$ when $V_{in} = 400$ V and $V_o = 50$ V. (a) At 500 W. (b) At 1 kW.

Fig. 12 shows the dynamic performance of the proposed control strategy. In this figure, the output load changes from 1 kW to 500 W and finally returns to 1 kW when the input voltage $V_{in}$ is 400 V and the output voltage $V_o$ is 50 V. As shown in Fig. 12, the voltages of the two input capacitors $V_1$ and $V_2$ are all kept constant under the proposed control strategy when load changes.

Fig. 13 shows the efficiency curves with the various input voltages when the output voltage $V_o$ is 50 V. The maximum efficiency under the proposed control strategy is over 95%. As shown in Fig. 13, the efficiencies of the proposed control strategy are higher than those of the conventional control strategy. This outcome is consistent with the result of the theoretical analysis. Fig. 14 shows the calculated power loss distribution when input voltage $V_{in}$ is 400 V, output voltage $V_o$ is 50 V, and output power $P_o$ is 1 kW. The conduction loss of the auxiliary switches is decreased because of the reduced conduction losses in the free-wheeling periods under the proposed control strategy. Such reduction improves the efficiency of converters. The increased efficiency under the proposed control strategy becomes particularly evident with increasing input power.
auxiliary switches are reduced, and the efficiency of converters can be effectively increased under the proposed control strategy compared with the conventional control strategy. The operation principles and performances of the proposed control strategy are analyzed in detail. Finally, the effectiveness and feasibility of the proposed control strategy are verified through the simulation and experimental results.

**APPENDIX**

**TABLE II**

<table>
<thead>
<tr>
<th>Component Description</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main Switches $S_1$ and $S_2$</td>
<td>IPW60R041C6</td>
</tr>
<tr>
<td>Auxiliary Switches $S_3$ and $S_4$</td>
<td>IRFP4868PBF</td>
</tr>
<tr>
<td>Output Rectifier Diodes $D_1$–$D_4$</td>
<td>MBR40250TG</td>
</tr>
<tr>
<td>Turns Ratio of the Transformer $T_r$</td>
<td>20:12</td>
</tr>
<tr>
<td>Leakage Inductance $L_r$ (µH)</td>
<td>24</td>
</tr>
<tr>
<td>Input Capacitors $C_1$ and $C_2$ (µF)</td>
<td>100</td>
</tr>
<tr>
<td>Output Filter Inductor $L_o$ (µH)</td>
<td>140</td>
</tr>
<tr>
<td>Output Filter Capacitor $C_o$ (µF)</td>
<td>470</td>
</tr>
<tr>
<td>Switching Frequency (kHz)</td>
<td>50</td>
</tr>
<tr>
<td>Dead Time ($\mu S$)</td>
<td>400</td>
</tr>
</tbody>
</table>

**REFERENCES**


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