JPE

Reduced-order Mapping and Design-oriented Instability for Constant On-time Current-mode Controlled Buck Converters with a PI Compensator

Xi Zhang*, Jianping Xu*, Jiahui Wu*, Bocheng Bao**, Guohua Zhou†, and Kaitun Zhang*

*,†Key Laboratory of Magnetic Suspension Technology and Maglev Vehicle, Ministry of Education, School of Electrical Engineering, Southwest Jiaotong University, Chengdu, China
**School of Information Science and Engineering, Changzhou University, Changzhou, China

Abstract

The constant on-time current-mode controlled (COT-CMC) switching dc-dc converter is stable, with no subharmonic oscillation in its current loop when a voltage ripple in its outer voltage loop is ignored. However, when its output capacitance is small or its feedback gain is high, subharmonic oscillation may occur in a COT-CMC buck converter with a proportional-integral (PI) compensator. To investigate the subharmonic instability of COT-CMC buck converters with a PI compensator, an accurate reduced-order asynchronous-switching map model of a COT-CMC buck converter with a PI compensator is established. Based on this, the instability behaviors caused by output capacitance and feedback gain are investigated. Furthermore, an approximate instability condition is obtained and design-oriented stability boundaries in different circuit parameter spaces are yielded. The analysis results show that the instability of COT-CMC buck converters with a PI compensator is mainly affected by the output capacitance, output capacitor equivalent series resistance (ESR), feedback gain, current-sensing gain and constant on-time. The study results of this paper are helpful for the circuit parameter design of COT-CMC switching dc-dc converters. Experimental results are provided to verify the analysis results.

Key words: constant on-time current-mode control (COT-CMC), Buck converter, proportional-integral (PI) compensator, reduced-order mapping, instability

I. INTRODUCTION

The current-mode control (CMC) architecture for switching dc-dc converters has been widely used in various applications [1]-[6]. The CMC architecture has two feedback loops, an inner current loop and an outer voltage loop. Typically, an inductor current is used as the control variable in the inner current loop, whereas an error amplifier with its corresponding proportional-integral (PI) compensator is used in the outer voltage loop when the effect of the zero introduced by the output capacitor equivalent series resistance (ESR) can be neglected [7]. There are two different current-mode control architectures, the constant-frequency current-mode control (CF-CMC) and the variable-frequency current-mode control (VF-CMC) [8], where the CF-CMC includes a peak-current-mode control and a valley-current-mode control, and the VF-CMC includes a constant on-time current-mode control (COT-CMC), a constant off-time current-mode control and a hysteresis current-mode control [2].

The instabilities and dynamical behaviors of CF-CMC switching dc-dc converters have been widely studied [9]-[26]. Subharmonic oscillation exists in the current loop of switching dc-dc converters with the peak-current-mode control when $d > 50\%$ (or with the valley-current-mode control when $d < 50\%$) [2]. For the prediction of instability and optimal designs of a CF-CMC switching dc-dc converter, various modeling and

analysis methods, such as discrete-time modeling [10], sampled-data modeling [11], and other improved modeling and analysis methods [12], [13], have been proposed. However, when the effect of voltage ripple in the outer voltage loop cannot be ignored, the operation range of the subharmonic oscillation is enlarged in CF-CMC buck converters [9], [25], whereas the operation range of the subharmonic oscillation is reduced in CF-CMC boost-like converters [26].

Furthermore, by using dynamical analysis methods based on bifurcation theory, some complex nonlinear behaviors, such as chaos [15], [16], coexisting fast-scale and slow-scale instability [17], [18], missed switching phenomenon [19], and symmetrical dynamics [20], are revealed. Then the operation-state region classifications and instability boundaries are obtained [21]-[23]. This is helpful for the comprehensive understanding of the dynamical behaviors and to design the circuit parameters of CF-CMC switching dc-dc converters.

Compared with conventional voltage-mode control, the CF-CMC provides better transient performance by replacing the saw-tooth waveform with an inductor current ripple as a modulation ramp [1]. However, ramp compensation is usually required in the feedback control loop of CF-CMC switching dc-dc converters to eliminate subharmonic oscillations [2], which lowers the transient performance of the converters [14].

When the voltage ripple of the outer voltage loop can be neglected, there is no subharmonic oscillation in the current-loop of VF-CMC switching dc-dc converters [8], [27], [28]. Without ramp compensation, VF-CMC can obtain better transient performance by designing a higher gain bandwidth [9]. Thus, VF-CMC is an alternative to CF-CMC to avoid subharmonic oscillations in the current loop [8]. However, it should be pointed out that when the feedback gain of the outer voltage loop of VF-CMC switching dc-dc converters is high enough, the outer loop voltage ripple cannot be ignored, which leads to the occurrence of subharmonic oscillations [9].

COT-CMC has been widely used to improve the light-load efficiency in various applications, such as voltage regulator modules (VRMs) and point of load (POL) converters [5], [6], [29]-[31]. It is observed that when an output capacitor with a small capacitance, such as a ceramic capacitor, is utilized, subharmonic oscillations also occurs in COT-CMC buck converters. However, there has been no detailed analysis of the subharmonic instability in COT-CMC buck converters so far.

The describing function method is widely used to investigate small-signal characteristics and open-loop stability for VF-CMC switching dc-dc converters [8], [27], [30], [31]. However, the effect of the voltage ripple of the outer voltage loop on the stability of the converter is not included in these models. Recently, discrete-time modeling and Floquet theory have been used to analyze the closed-loop stability of constant-frequency ripple-based control buck converters [32]. However, COT-CMC is a kind of variable-frequency control, with no clock signal. Thus, its discrete-time model is an asynchronous-switching map model, which is similar to that of the voltage ripple-based COT control and fixed off-time (FOT) control buck converters [33], [34].

The COT control and FOT control buck converters reported in [33] and [34] are second-order circuits. However, a COT-CMC buck converter with a PI compensator is a third-order circuit. In this paper, by considering that the compensation capacitor voltage in a PI compensator is a linear combination of the inductor current and the output capacitor voltage, an accurate reduced-order asynchronous-switching map model of a COT-CMC buck converter with a PI compensator is established. Based on the model, a design-oriented stability analysis of the circuit parameters has been performed. Furthermore, the critical condition for subharmonic instability is obtained by using an approximate asynchronous-switching map model. This is helpful to understand the instability behaviors and to design the circuit parameters of VF-CMC switching dc-dc converters.

This paper is organized as follows. Section II elaborates on the operational principle of a COT-CMC buck converter with a PI compensator operating in the continuous conduction mode (CCM) as well as the subharmonic oscillation phenomenon caused by an output capacitor with a small capacitance or a PI compensator with a high feedback gain. In Section III, by using two-order state equations in two switch states, a reduced-order piecewise smooth continuous model is described. Furthermore, an accurate reduced-order asynchronous-switching map model is established, and the dynamic behaviors with variations of the output capacitance and feedback gain are investigated. In Section IV, an approximate critical instability condition is derived, and four stability boundaries in four different circuit parameter spaces are yielded. In Section V, a hardware experimental prototype is provided to verify the theoretical analysis results. Some conclusions are summarized in Section VI.

II. Subharmonic Oscillation in a COT-CMC Buck Converter with a PI Compensator

A. COT-CMC Buck Converter with a PI Compensator

The schematic diagram of a COT-CMC buck converter with a PI compensator is shown in Fig. 1(a). Its power stage consists of an input voltage source V_{in}, a switch S, a diode D, an inductor L, an output capacitor C with an ESR r, and a load resistor R. The COT-CMC controller consists of a current-sensing circuit with a gain R_s, a PI compensator, a comparator, an RS trigger and an ON-Timer.

The output voltage $v_o(t)$ of the COT-CMC buck converter can be expressed as:

$$v_o(t) = \kappa[ri_L(t) + v_C(t)] \tag{1}$$

where $\kappa = R/(R+r)$, and $i_L(t)$ and $v_C(t)$ are the inductor current and output capacitor voltage, respectively.

The control signal $v_{con}(t)$ can be deduced as:

$$v_{con}(t) = (1+g)V_{ref} - gv_o(t) - v_a(t) \quad (2)$$

where V_{ref} is the reference voltage, $g = R_a/R_{in}$ is the feedback gain of the PI compensator, and v_a is the compensation capacitor voltage.

A COT-CMC buck converter with a PI compensator is a structure-varying and piecewise-linear dynamic system. Fig. 1(b) shows its key steady-state operation waveforms when operating in the CCM, where v_o and V_o are the instantaneous

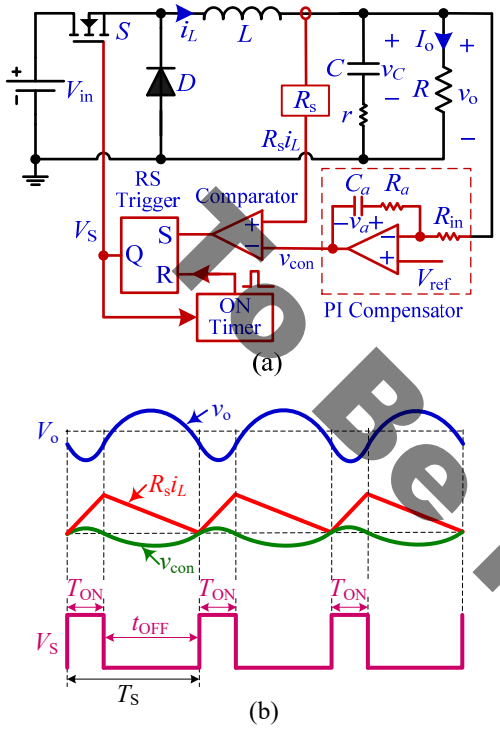


Fig. 1. COT-CMC buck converter with PI compensator. (a) Circuit schematic diagram. (b) Key operation waveforms.

output voltage and the averaged output voltage, V_S is the control pulse voltage, T_{ON} is the constant on-time interval, t_{OFF} is the off-time interval modulated by the sensed inductor current $R_s i_L$ and the control signal v_{con}, and T_S is the switching cycle.

For a COT-CMC buck converter operating in the CCM, its operation can be identified as [17]:

Switch state 1: switch S is on and diode D is off

Switch state 2: switch S is off and diode D is on

In switch state 1, switch S is turned on and $R_s i_L$ increases. After a preset on-time T_{ON}, switch S is turned off, the converter enters switch state 2 from switch state 1, and $R_s i_L$ decreases. Once $R_s i_L$ decreases to v_{con}, switch S is turned on again, and a new switching cycle is initiated. Therefore, the switched condition of the converter can be written as:

$$R_s i_L(t) = v_{con}(t) \quad (3)$$

B. Subharmonic Oscillation Phenomenon

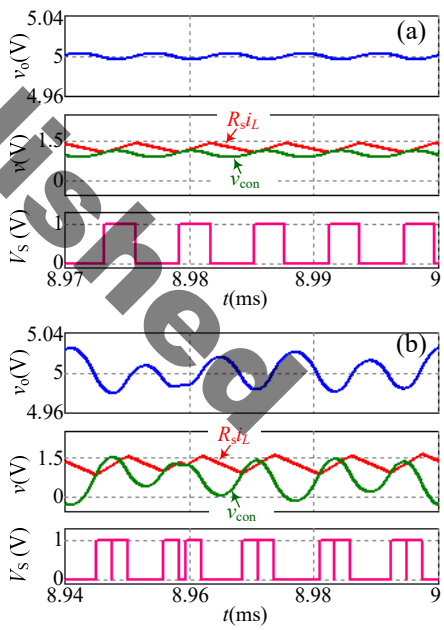
In general, when the voltage ripple of an outer voltage loop can be ignored, a COT-CMC buck converter with a PI compensator operates in stable operation [8], [27], [28]. However, when the capacitance of an output capacitor is small or the feedback gain is high, a large voltage ripple exists in the outer voltage loop, which causes subharmonic oscillation.

To show subharmonic oscillation in a COT-CMC buck converter with a PI compensator, typical circuit parameters as listed in Table I are designed. Fig. 2 shows simulation results under different output capacitances and feedback gains, while Fig. 2(a) shows simulation results with typical circuit

TABLE I

TYPICAL CIRCUIT PARAMETERS OF A COT-CMC BUCK CONVERTER WITH A PI COMPENSATOR

Parameters	Significations	Values
V_{in}	Input voltage	12 V
L	Inductance	50 μH
C	Output capacitance	47 μF
r	Output capacitor ESR	5 mΩ
R	Load resistance	4 Ω
V_{ref}	Reference voltage	5 V
g	Feedback gain of PI compensator	40
C_a	Compensation capacitance	10 nF
R_s	Current-sensing gain	1 V/A
T_{ON}	Constant on-time	2.5 μs



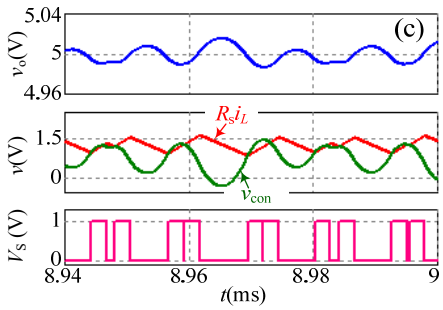


Fig. 2. Stable operation and subharmonic oscillation in a COT-CMC buck converter with a PI compensator: (a) C = 47 μF and g = 40, stable operation; (b) C = 30 μF and g = 40, subharmonic oscillation; (c) C = 47 μF and g = 60, subharmonic oscillation.

parameters as listed in Table I. This shows that the converter operates in a stable state. However, when C = 30 μF or g = 60 and the other circuit parameters are as listed in Table I, the converter operates with subharmonic oscillation, which produces a large inductor current ripple and an output voltage ripple, as shown in Figs. 2(b) and 2(c). In addition, as observed in Figs. 2(b) and 2(c), when subharmonic oscillation occurs in the converter, two successive control pulses frequently appear in the control pulse train, which implies the occurrence of a pulse bursting phenomenon [35].

As shown in Fig. 2(a), if the capacitance of the output capacitor is large enough or if the gain of the PI compensator is low enough, the slope of the control signal $v_{con}(t)$ becomes smaller than or equal to that of $R_s i_L$ when switch S is turned on. Thus, $v_{con}(t)$ is always lower than $R_s i_L$ in the on-time interval, and the normal operation of the COT-CMC buck converter with a PI compensator can be ensured. On the other hand, as shown in Figs. 2(b) and 2(c), if the capacitance of an output capacitor is small enough or if the gain of a PI compensator is high enough, the slope of $v_{con}(t)$ becomes larger than that of $R_s i_L$ when switch S is turned on. Then the COT-CMC buck converter with a PI compensator operates abnormally and its stability is lost. Consequently, subharmonic oscillation in this kind of converter is obviously associated with the capacitance of the output capacitor, the feedback gain, and the current-sensing gain. Additionally, considering that $v_{con}(t)$ is related to g, $v_o(t)$ and $v_a(t)$, subharmonic oscillation may depend on other circuit parameters, such as r, κ, T_{ON}, etc.

In the following sections of this paper, reduced-order asynchronous-switching mapping is considered to elaborate instability behaviors and dynamic mechanisms. In addition, the approximate critical instability condition is used to study the design-oriented stability boundaries for circuit parameters.

III. Accurate Reduced-order Asynchronous -switching Map and Dynamic Behavior

A. Reduced-order Piecewise Smooth Continuous Model

The converter shown in Fig. 1(a) has three state variables. These variables are the inductor current i_L, output capacitor voltage v_C and compensation capacitor voltage v_a. For a COT-CMC buck converter with a PI compensator, the power stage can be described by two-order state equations in two switch states, which are:

$$\dot{\mathbf{x}}(t) = \mathbf{A}_m \mathbf{x}(t) + \mathbf{B}_m V_{\text{in}} \quad (t_{m-1} \le t < t_m,\ m = 1,2) \tag{4}$$

where $\mathbf{x}(t) = [i_L(t)\ v_C(t)]^T$, m represents the m-th switch state, t_{m-1} and t_m denote the time instants at the beginning and end of the m-th switch state, and the matrices **A**'s and **B**'s are expressed as:

$$\mathbf{A}_1 = \mathbf{A}_2 = \begin{bmatrix} -\dfrac{\kappa r}{L} & -\dfrac{\kappa}{L} \\ \dfrac{\kappa}{C} & -\dfrac{\kappa}{RC} \end{bmatrix},\quad \mathbf{B}_1 = \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix},\quad \mathbf{B}_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}.$$

In a COT-CMC buck converter with a PI compensator, the transition between two switch states is decided by a COT-CMC controller. For the PI compensator of the outer voltage loop as shown in Fig. 1(a), the compensation capacitor voltage $v_a(t)$ in the m-th switch state is:

$$v_a(t) = v_a(t_{m-1}) + \frac{g}{\tau_a}\int_{t_{m-1}}^{t} v_o(\tau)\mathrm{d}\tau - \frac{gV_{\text{ref}}}{\tau_a}(t - t_{m-1}) \tag{5}$$

where $\tau_a = R_a C_a$ is the time constant of the PI compensator.

According to (1) and (4), the output voltage $v_o(t)$ in the m-th switch state can be expressed as $v_o(t) = L\mathbf{F}\left[\mathbf{B}_m V_{\text{in}} - \dot{\mathbf{x}}(t)\right]$, where $\mathbf{F}$ = [1 0]. Thus, in the m-th switch state, by substituting $v_o(t)$ into (5), $v_a(t)$ can be unified as:

$$\begin{aligned} v_a(t) = v_a(t_{m-1}) &+ \frac{g}{\tau_a}(L\mathbf{F}\mathbf{B}_m V_{\text{in}} - V_{\text{ref}})(t - t_{m-1}) \\ &- \frac{g}{\tau_a} L\mathbf{F}\left[\mathbf{x}(t) - \mathbf{x}(t_{m-1})\right] \end{aligned} \tag{6}$$

From (6), it is known that v_a is a linear combination of i_L and v_C. Thus, a reduced-order piecewise smooth continuous model of the COT-CMC buck converter with a PI compensator can be represented by state equations (4).

B. Accurate Reduced-order Asynchronous-switching Map Model

When a COT-CMC buck converter with a PI compensator operates in the m-th switch state, its corresponding operation time interval is $\tau_m = t_m - t_{m-1}$. Let $\mathbf{x}(t_{m-1})$ denote the state variable at the time instant t_{m-1}. Then from (4), the state variable at the time instant t_m can be solved as:

$$\mathbf{x}(t_m) = \mathbf{P}_m(\tau_m)\mathbf{x}(t_{m-1}) + \mathbf{Q}_m(\tau_m)V_{\text{in}} \quad (m = 1,2) \tag{7}$$

where:

$$\mathbf{P}_m(\tau_m)=\begin{bmatrix} a_m+\frac{\beta}{\omega}b_m & -\frac{\kappa}{\omega L}b_m \\ \frac{\kappa}{\omega C}b_m & a_m-\frac{\beta}{\omega}b_m \end{bmatrix},$$

$$\mathbf{Q}_1(\tau_1)=\begin{bmatrix} \frac{1}{R}-\frac{1}{R}a_1+\frac{R-\alpha L}{\omega RL}b_1 \\ 1-a_1-\frac{\alpha}{\omega}b_1 \end{bmatrix},\quad \mathbf{Q}_2(\tau_2)=\begin{bmatrix}0\\0\end{bmatrix},$$

$$\alpha=\frac{\kappa}{2}\left(\frac{1}{RC}+\frac{r}{L}\right),\quad \beta=\frac{\kappa}{2}\left(\frac{1}{RC}-\frac{r}{L}\right),\quad \omega=\sqrt{\frac{\kappa}{LC}-\alpha^2},$$

$$a_m=\cos\omega\tau_m e^{-\alpha\tau_m},\quad b_m=\sin\omega\tau_m e^{-\alpha\tau_m}.$$

The main operation waveforms of a COT-CMC buck converter with a PI compensator in the n-th switching cycle are shown in Fig. 3. In Fig.3, $\mathbf{x}_n=[i_{L,n},\ v_{C,n}]^T$, $v_{a,n}$ and $v_{\mathrm{con},n}$ are the sampling values of $\mathbf{x}=[i_L,\ v_C]^T$, v_a and v_{con} at the beginning of the n-th control pulse, respectively. $\mathbf{x}_{n+1}=[i_{L,n+1},\ v_{C,n+1}]^T$, $v_{a,n+1}$ and $v_{\mathrm{con},n+1}$ are the sampling values of $\mathbf{x}=[i_L,\ v_C]^T$, v_a and v_{con} at the beginning of the $(n+1)$-th control pulse, respectively. Meanwhile $\mathbf{x}(t_1)=[i_L(t_1),\ v_C(t_1)]^T$ and $v_a(t_1)$ are the sampling values of $\mathbf{x}=[i_L,\ v_C]^T$ and v_a at the falling edge of the n-th constant on-time control pulse, respectively.

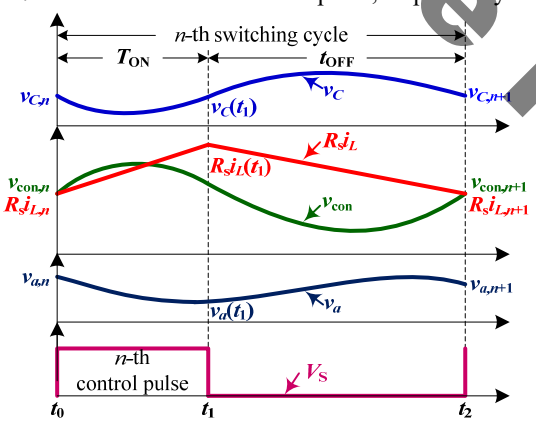


Fig. 3. Main steady-state operation waveforms in the n-th switching cycle.

In the n-th switching cycle, for switch state 1, *i.e.* when switch S is on and diode D is off, $\mathbf{x}_n$ is the initial state variable, and the operation time interval $\tau_1=t_1-t_0$ is preset as T_{ON}. According to (6) and (7), the state variable $\mathbf{x}(t_1)$ and the corresponding compensation capacitor voltage $v_a(t_1)$ are:

$$\mathbf{x}(t_1)=\begin{bmatrix} i_L(t_1) & v_C(t_1)\end{bmatrix}=\mathbf{P}_1(T_{\mathrm{ON}})\mathbf{x}_n+\mathbf{Q}_1(T_{\mathrm{ON}})V_{\mathrm{in}} \tag{8a}$$

and:

$$v_a(t_1)=v_{a,n}+\frac{g}{\tau_a}(L\mathbf{F}\mathbf{B}_1V_{\mathrm{in}}-V_{\mathrm{ref}})T_{\mathrm{ON}}-\frac{g}{\tau_a}L\mathbf{F}[\mathbf{x}(t_1)-\mathbf{x}_n] \tag{8b}$$

For switch state 2, *i.e.* when switch S is off and diode D is on, $\mathbf{x}(t_1)$ is the initial state variable, and the operation time interval is $\tau_2=t_2-t_1=t_{\mathrm{OFF}}$. According to (6) and (7), at the beginning of the $(n+1)$-th control pulse, the state variable $\mathbf{x}_{n+1}$ and the corresponding compensation capacitor voltage $v_{a,n+1}$ are given as:

$$\mathbf{x}_{n+1}=\mathbf{P}_2(t_{\mathrm{OFF}})\mathbf{x}(t_1) \tag{9a}$$

and:

$$v_{a,n+1}=v_a(t_1)+\frac{g}{\tau_a}(L\mathbf{F}\mathbf{B}_2V_{\mathrm{in}}-V_{\mathrm{ref}})t_{\mathrm{OFF}}-\frac{g}{\tau_a}L\mathbf{F}\left[\mathbf{x}_{n+1}-\mathbf{x}(t_1)\right] \tag{9b}$$

where t_{OFF} can be obtained by numerically solving the following transcendental equation:

$$\begin{aligned} R_{\mathrm{s}}\mathbf{F}\mathbf{x}_{n+1}&=v_{\mathrm{con},n+1}\\ &=(1+g)V_{\mathrm{ref}}-g\kappa(ri_{L,n+1}+v_{C,n+1})-v_{a,n+1}\end{aligned} \tag{10}$$

Consequently, an accurate reduced-order asynchronous-switching map model of the COT-CMC buck converter with a PI compensator can be given as:

$$\mathbf{x}_{n+1}=\mathbf{P}_2(t_{\mathrm{OFF}})\left[\mathbf{P}_1(T_{\mathrm{ON}})\mathbf{x}_n+\mathbf{Q}_1(T_{\mathrm{ON}})V_{\mathrm{in}}\right] \tag{11}$$

From (11), the Jacobian can be obtained as:

$$\mathbf{J}_n=\begin{bmatrix} J_{11} & J_{12}\\ J_{21} & J_{22}\end{bmatrix} \tag{12}$$

where $J_{11}=\frac{\partial i_{L,n+1}}{\partial i_{L,n}}$, $J_{12}=\frac{\partial i_{L,n+1}}{\partial v_{C,n}}$, $J_{21}=\frac{\partial v_{C,n+1}}{\partial i_{L,n}}$ and $J_{22}=\frac{\partial v_{C,n+1}}{\partial v_{C,n}}$ are given in the Appendix.

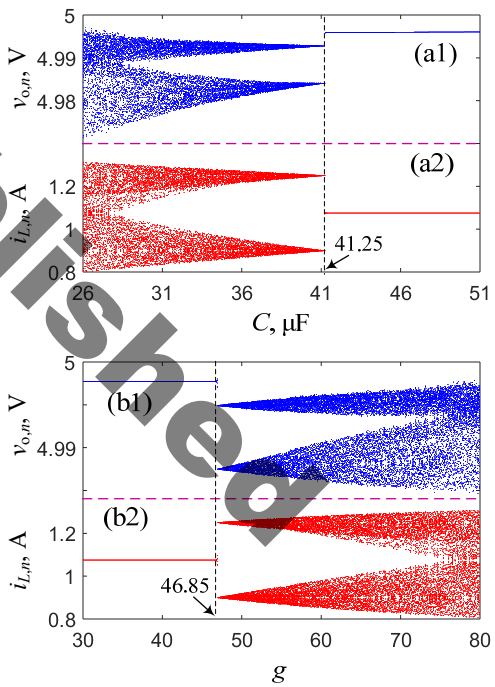


Fig. 4. Dynamic behaviors with: (a) C decreasing: (b) g increasing, where $v_{\mathrm{o},n}$ and $i_{L,n}$ are the output voltage v_{o} and inductor current i_L at the beginning of each control pulse, respectively.

The eigenvalues of the Jacobian in (12) can be obtained by solving the characteristic equation in λ:

$$\det\left|\lambda\mathbf{1}-\mathbf{J}_n\right|=0 \tag{13}$$

From (12), the solutions of (13) can be solved as:

$$\lambda_1=0 \text{ and } \lambda_2=J_{11}+J_{22} \tag{14}$$

Since $\lambda_1 = 0$ is always located in a unit circle, the stability of the COT-CMC buck converter with a PI compensator is determined by the location of λ_2.

C. Dynamic Behaviors with Variations of the Output Capacitance and Feedback Gain

Based on an accurate reduced-order asynchronous-switching map model (11) and its Jacobian (12), the dynamical behaviors of a COT-CMC buck converter with a PI compensator with variations of the output capacitance and feedback gain can be investigated.

For typical circuit parameters, as listed in Table I, and initial state variables $\mathbf{x}_0 = [0, 0]^T$ and $v_{a,0} = 0$, bifurcation diagrams of $i_{L,n}$ and $v_{o,n}$ with respect to the output capacitance C and feedback gain g are depicted in Figs. 4(a) and 4(b), respectively. With a decrease of C or an increase of g, the period-doubling bifurcations occur at C = 41.25 μF or g = 46.85, and the converter abruptly enters the chaotic operation state from the period-1 oscillation state, leading to the occurrence of instability.

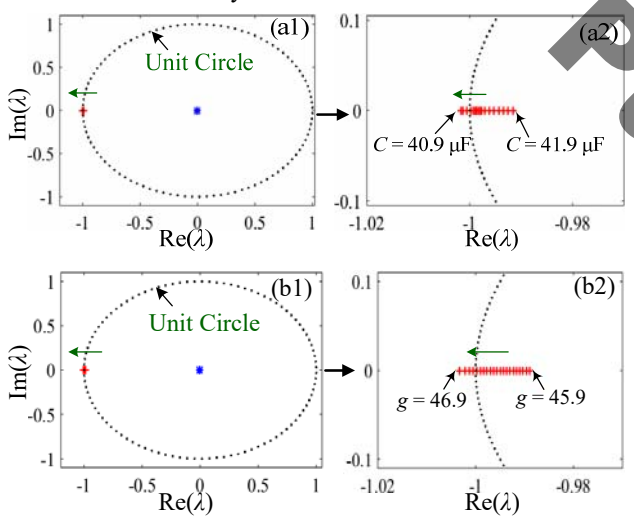


Fig. 5. Loci of two eigenvalues for the converter, where "*" and "+" denote λ_1 and λ_2, respectively: (a) C decreasing from 41.9 μF to 40.9 μF; (b) g increasing from 45.9 to 46.9; (a2) and (b2) are close-up views of the eigenvalue λ_2 in (a1) and (b1).

Additionally, the loci of two eigenvalues with a decrease of C or an increase of g are depicted in Fig. 5, where λ_1 is always located in the unit circle and λ_2 leaves the unit circle via –1 with C decreasing from 41.9 μF to 40.9 μF or g increasing from 45.9 to 46.9, which implies that the converter is out of stable operation.

Obviously, the circuit parameters, including the output capacitance and feedback gain, have a significant effect on the stability of the COT-CMC buck converter with a PI compensator, i.e., subharmonic oscillation occurs when the output capacitance is small or the feedback gain is high.

IV. Approximate Critical Instability Condition and Stability Boundary

The accurate model (11) derived in Section III is infeasible for deriving the explicit expressions of its Jacobi matrix and it is not convenient to design the circuit parameters of the COT-CMC buck converter with a PI compensator. In this section, an approximate reduced-order asynchronous-switching map model is established. A design-oriented closed-loop instability condition is obtained from this model.

A. Approximate Critical Instability Condition

Compared with the averaged output voltage, the ripple of the output voltage is small and can be ignored. Thus, both the increase in slope $m_1 = (V_{in} – V_o)/L$ and the decrease in slope $–m_2 = –V_o/L$ of the inductor current can be approximated as constants in each switching cycle.

In the n-th switching cycle, as shown in Fig. 3, the inductor current $i_L(t)$, output capacitor voltage $v_C(t)$ and compensation capacitor voltage $v_a(t)$ at $t = t_1$ and $t = t_2$ are approximated as:

$$i_L(t_1)=i_{L,n}+m_1T_{ON} \tag{15a}$$

$$v_C(t_1)=v_{C,n}+\frac{i_{L,n}-I_o}{C}T_{ON}+\frac{m_1}{2C}T_{ON}^2 \tag{15b}$$

$$v_a(t_1)=v_{a,n}+\frac{g}{\tau_a}(V_{in}-V_{ref})T_{ON}-\frac{g}{\tau_a}L[i_L(t_1)-i_{L,n}] \tag{15c}$$

and:

$$i_L(t_2)=i_{L,n+1}=i_L(t_1)-m_2t_{OFF} \tag{16a}$$

$$v_C(t_2)=v_{C,n+1}=v_C(t_1)+\frac{i_L(t_1)-I_o}{C}t_{OFF}-\frac{m_2}{2C}t_{OFF}^2 \tag{16b}$$

$$v_a(t_2)=v_{a,n+1}=v_a(t_1)-\frac{g}{\tau_a}V_{ref}t_{OFF}-\frac{g}{\tau_a}L\left[i_{L,n+1}-i_L(t_1)\right] \tag{16c}$$

where $I_o = V_o/R$ stands for the averaged output current.

The time interval t_{OFF} of switch state 2 in (16) can be obtained by substituting (15) and (16) into (10), which gives rise to:

$$\begin{aligned}&\frac{g\kappa m_2}{2C}t_{OFF}^2+\left[(R_s+g\kappa r)m_2-\frac{g\kappa}{C}(i_{L,n}+m_1T_{ON}-I_o)\right]t_{OFF}\\&=(R_s+g\kappa r)(i_{L,n}+m_1T_{ON})+g\kappa(v_{C,n}+\frac{i_{L,n}-I_o}{C}T_{ON}+\frac{m_1}{2C}T_{ON}^2)\\&+v_{a,n}-(1+g)V_{ref}\end{aligned} \tag{17}$$

It is noted that t_{OFF} is not a constant but a variable time interval. Substituting (15a) and (15b) into (16a) and (16b), an approximate reduced-order asynchronous-switching map model of the COT-CMC buck converter with a PI compensator is summarized as:

$$\begin{cases}i_{L,n+1}=i_{L,n}+m_1T_{ON}-m_2t_{OFF}\\v_{C,n+1}=v_{C,n}+\dfrac{T_{ON}+t_{OFF}}{C}(i_{L,n}-I_o)+\dfrac{m_1T_{ON}^2}{2C}+\dfrac{m_1T_{ON}t_{OFF}}{C}-\dfrac{m_2t_{OFF}^2}{2C}\end{cases}$$

(18)

By substituting (18) into (12), the Jacobian for the approximate model (18) can be calculated as:

$$\mathbf{J}_n = \begin{bmatrix} 1-m_2\dfrac{\partial t_{\mathrm{OFF}}}{\partial i_{L,n}} & -m_2\dfrac{\partial t_{\mathrm{OFF}}}{\partial v_{C,n}} \\ \dfrac{T_{\mathrm{ON}}+t_{\mathrm{OFF}}}{C}+\gamma\dfrac{\partial t_{\mathrm{OFF}}}{\partial i_{L,n}} & 1+\gamma\dfrac{\partial t_{\mathrm{OFF}}}{\partial v_{C,n}} \end{bmatrix} \tag{19}$$

where:

$$\gamma = \frac{i_{L,n}-I_{\mathrm{o}}+m_1T_{\mathrm{ON}}-m_2t_{\mathrm{OFF}}}{C}$$

From (17), $\dfrac{\partial t_{\mathrm{OFF}}}{\partial i_{L,n}}$ and $\dfrac{\partial t_{\mathrm{OFF}}}{\partial v_{C,n}}$ in (19) can be obtained as:

$$\frac{\partial t_{\mathrm{OFF}}}{\partial i_{L,n}} = \frac{(R_{\mathrm{s}}+g\kappa r)C+g\kappa(T_{\mathrm{ON}}+t_{\mathrm{OFF}})}{m_2(g\kappa r+R_{\mathrm{s}})C-g\kappa(i_{L,n}-I_{\mathrm{o}}+m_1T_{\mathrm{ON}}-m_2t_{\mathrm{OFF}})} \tag{20a}$$

$$\frac{\partial t_{\mathrm{OFF}}}{\partial v_{C,n}} = \frac{g\kappa C}{m_2(R_{\mathrm{s}}+g\kappa r)C-g\kappa(i_{L,n}-I_{\mathrm{o}}+m_1T_{\mathrm{ON}}-m_2t_{\mathrm{OFF}})} \tag{20b}$$

In the neighborhood of the instability boundary, there exist the following approximate conditions:

$$i_{L,n} \approx I_{\mathrm{o}}-0.5m_1t_{\mathrm{ON}}, \quad t_{\mathrm{OFF}} \approx m_1T_{\mathrm{ON}}/m_2 \tag{21}$$

By substituting (20) and (21) into (19), two eigenvalues of (19) can be written as:

$$\lambda_1 = 0 \quad \text{and} \quad \lambda_2 = \frac{2m_2(g\kappa r+R_{\mathrm{s}})C-g\kappa(2m_2+m_1)T_{\mathrm{ON}}}{2m_2(g\kappa r+R_{\mathrm{s}})C+g\kappa m_1T_{\mathrm{ON}}} \tag{22}$$

To ensure that the COT-CMC buck converter operates in a stable state, it is necessary that both eigenvalues are inside the unit circuit, i.e., $|\lambda_2| < 1$. Thus, an approximate instability condition is:

$$2rC > T_{\mathrm{ON}} \tag{23a}$$

or:

$$2rC < T_{\mathrm{ON}} \quad \text{and} \quad g < g_{\mathrm{critical}} = \frac{2R_{\mathrm{s}}C}{\kappa(T_{\mathrm{ON}}-2rC)} \tag{23b}$$

where g_{critical} is the instability boundary of the feedback gain when $2rC < T_{\mathrm{ON}}$, which can also be derived using the harmonic balance analysis reported in [36].

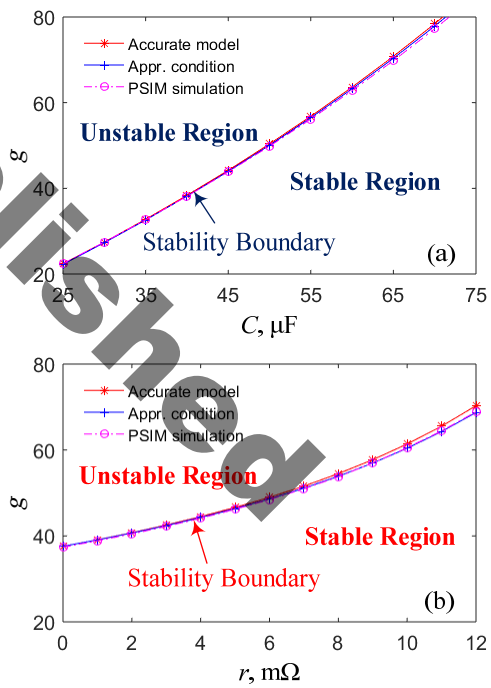
The result of (23) indicates that when $2rC > T_{\mathrm{ON}}$, the converter is always stable. However, when $2rC < T_{\mathrm{ON}}$, the converter is stable if $g < g_{\mathrm{critical}}$, otherwise it is unstable. The instability of the COT-CMC buck converter with a PI compensator is affected by the output capacitance, output capacitor ESR, feedback gain, load resistance, current-sensing gain and constant on-time. Additionally, when compared with the load resistance, the output capacitor ESR is very small, i.e., $\kappa = R/(R+r) \approx 1$. Then the effect of the load resistance on the stability of the COT-CMC buck converter can be ignored.

B. Stability Boundary in the Circuit Parameter Space

For typical circuit parameters, as listed in Table I, based on the approximate critical instability condition (23b), the stability boundaries between the stable and unstable operation regions in four different circuit parameter spaces, including C-g, r-g, R_{s}-g and T_{ON}-g, are plotted in Figs. 6(a), 6(b), 6(c), and 6(d), respectively. They are denoted as 'Appr. Condition'. The approximate critical instability boundaries between the stable and unstable operation regions are simultaneously verified by MATLAB numerical simulations based on the accurate map model (11) (denoted as 'Accurate model') and PSIM circuit simulations shown in Fig. 1 (denoted as 'PSIM simulation'). The results illustrate that the unstable operation regions are reduced with an increase of the output capacitance, output capacitor ESR and current-sensing gain or with a decrease of the feedback gain and constant on-time.

V. Experimental Verifications

To verify the above theoretical analysis results, an experimental prototype of the COT-CMC buck converter with a PI compensator is built. Taking the feedback gain g, output capacitance C, output capacitor ESR r, current-sensing gain R_{s} and constant on-time T_{ON} as adjustable circuit parameters, the other circuit parameters are listed in Table I. According to Fig. 6 and (23b), for eight sets of circuit



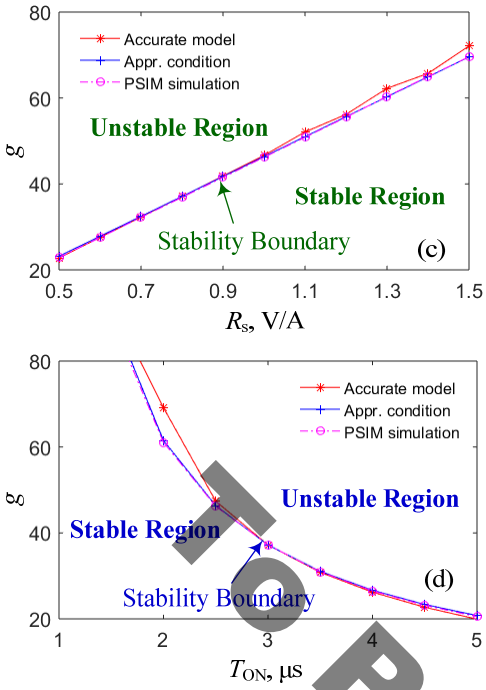


Fig. 6. Stability boundaries in: (a) the C-g space; (b) the r-g space; (c) the R_s-g space; (d) the T_{ON}-g space. The curve marked with "*" is simulated from the accurate map model (11), the curve marked with "+" is calculated from the approximate critical instability condition (21b), and the curve marked with "○" is plotted by a PSIM circuit simulation.

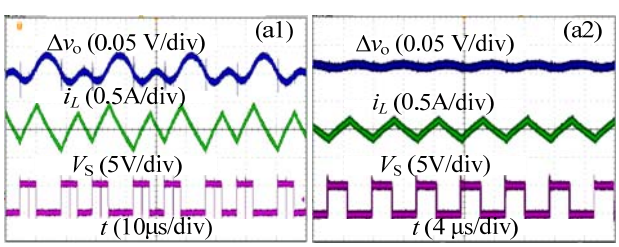
parameters g, C, r, R_s and T_{ON}, listed in Table II, the relations among g and $g_{critical}$, and the corresponding stability are obtained and summarized in Table II.

Fig. 7 shows experimental results for the different circuit parameters g, C, r, R_s and T_{ON} listed in Table II. From Fig. 7,

TABLE II

THEORETICAL RESULTS WITH DIFFERENT CIRCUIT PARAMETERS

No.	Adjustable circuit parameters	Relations of g and $g_{critical}$	Stability
a1	$g = 40$, $C = 30$ μF	$g > g_{critical} = 27.3$	Unstable
a2	$g = 40$, $C = 60$ μF	$g < g_{critical} = 63.2$	Stable
b1	$g = 60$, $r = 5$ mΩ	$g > g_{critical} = 46.4$	Unstable
b2	$g = 60$, $r = 11$ mΩ	$g < g_{critical} = 64.3$	Stable
c1	$g = 45$, $R_s = 0.6$ V/A	$g > g_{critical} = 27.8$	Unstable
c2	$g = 45$, $R_s = 1.3$ V/A	$g < g_{critical} = 60.3$	Stable
d1	$g = 35$, $T_{ON} = 4$ μs	$g > g_{critical} = 26.7$	Unstable
d2	$g = 35$, $T_{ON} = 2.5$ μs	$g < g_{critical} = 46.7$	Stable



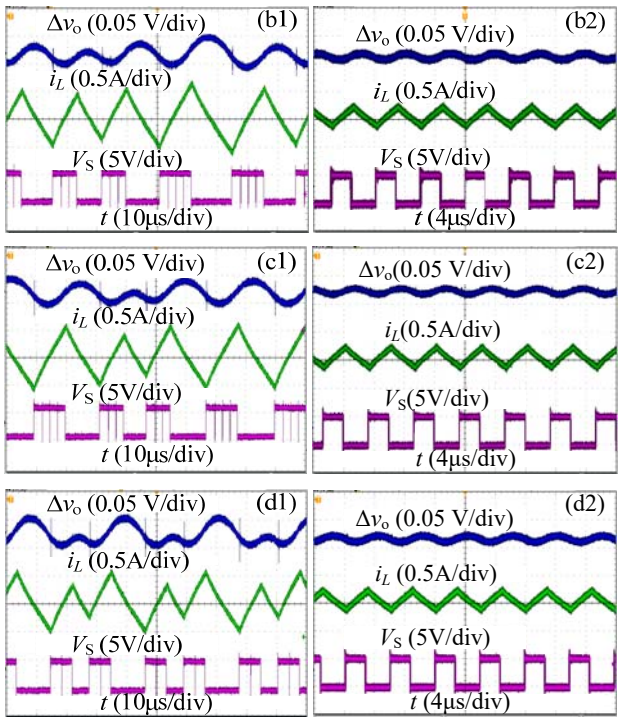


Fig. 7. Experimental results for different circuit parameters g, C, r, R_s and T_{ON} listed in Table II, where Δv_o, i_L and V_s denote output voltage ripple, inductor current and control pulse voltage, respectively.

it can be seen that when the output capacitance, output capacitor ESR and current-sensing gain are small, or when the constant on-time is large, the COT-CMC buck converter with a PI compensator operates in subharmonic oscillation with a large inductor current ripple and output voltage ripple. Otherwise, the converter operates in a stable period-1 state with a small inductor current ripple and an output voltage ripple. Obviously, these experimental results verify the theoretical analysis results in Table II. Specially, when subharmonic oscillation occurs, two or more successive control pulses may appear in the control pulse voltage, as observed from Figs. 7(a1), 7(b1), 7(c1) and 7(d1), which implies the occurrence of the pulse bursting phenomenon [35].

VI. CONCLUSIONS

When an output capacitor with a small capacitance or a PI compensator with a high feedback gain is used, the effect of the outer loop voltage ripple on the subharmonic oscillation in a COT-CMC buck converter with a PI compensator cannot be ignored. To investigate its instability mechanism, an accurate reduced-order asynchronous-switching map model is established and dynamic behaviors with variations of the output capacitance and feedback gain are analyzed. Furthermore, an approximate reduced-order asynchronous-

switching map model is built and an approximate critical instability condition is derived. Through numerical simulations of the accurate map model and the approximate critical instability condition along with PSIM circuit simulations, the stability boundaries between stable and unstable operation regions are simulated in four different circuit parameter spaces. The analysis and experimental results indicate that the instability is mainly affected by the output capacitance, output capacitor ESR, feedback gain and constant on-time. The unstable regions are reduced with an increase of the output capacitance, output capacitor ESR and current-sensing gain or a decrease of the feedback gain and constant on-time. The investigations in this paper provide a guideline for the circuit parameter selection of a COT-CMC buck converter in practical designs. It can also promote the fundamental theory development of VF-CMC switching dc-dc converters.

APPENDIX

Each of the elements of the Jacobian in (12) for the accurate model in (11) are derived as follows.

Let:

$$\xi_I = \beta a_2 - \alpha a_2 - \omega b_2 - \frac{\alpha\beta}{\omega} b_2 , \quad \xi_V = \frac{\kappa}{\omega L}(\alpha b_2 - \omega a_2) ,$$

$$\eta_+ = a_1 a_2 + \frac{\beta}{\omega}(a_1 b_2 + a_2 b_1) + \frac{\beta^2 LC - \kappa^2}{\omega^2 LC} b_1 b_2 ,$$

$$\rho_I = \frac{\kappa}{\omega C}(\omega a_2 - \alpha b_2) , \quad \rho_V = \frac{\alpha\beta}{\omega} b_2 - \omega b_2 - \alpha a_2 - \beta a_2 ,$$

$$\eta_- = a_1 a_2 - \frac{\beta}{\omega}(a_1 b_2 + a_2 b_1) + \frac{\beta^2 LC - \kappa^2}{\omega^2 LC} b_1 b_2 .$$

as well as:

$$\sigma_1 = \xi_I i_L(t_1) + \xi_V v_C(t_1) , \quad \sigma_2 = \rho_I i_L(t_1) + \rho_V v_C(t_1) .$$

Thus:

$$J_{11} = \sigma_1 \frac{\partial t_{\mathrm{OFF}}}{\partial i_{L,n}} + \eta_+ , \quad J_{12} = \sigma_1 \frac{\partial t_{\mathrm{OFF}}}{\partial v_{C,n}} - \frac{\kappa}{\omega L}(a_1 b_2 + a_2 b_1) ,$$

$$J_{21} = \sigma_2 \frac{\partial t_{\mathrm{OFF}}}{\partial i_{L,n}} + \frac{\kappa}{\omega C}(a_1 b_2 + a_2 b_1) , \quad J_{22} = \sigma_2 \frac{\partial t_{\mathrm{OFF}}}{\partial v_{C,n}} + \eta_- .$$

where:

$$\frac{\partial t_{\mathrm{OFF}}}{\partial i_{L,n}} = \frac{gL + \dfrac{g\kappa^2 \tau_a}{\omega C}(a_1 b_2 + a_2 b_1) + (g\kappa\tau_a r + \tau_a R_{\mathrm{s}} - gL)\eta_+}{gV_{\mathrm{ref}} - (g\kappa\tau_a r + \tau_a R_{\mathrm{s}} - gL)\sigma_1 - g\kappa\tau_a \sigma_2} ,$$

$$\frac{\partial t_{\mathrm{OFF}}}{\partial v_{C,n}} = \frac{g\kappa\tau_a \eta_- - \dfrac{\kappa}{\omega L}(g\kappa\tau_a r + \tau_a R_{\mathrm{s}} - gL)(a_1 b_2 + a_2 b_1)}{gV_{\mathrm{ref}} - (g\kappa\tau_a r + \tau_a R_{\mathrm{s}} - gL)\sigma_1 - g\kappa\tau_a \sigma_2} .$$

ACKNOWLEDGMENT

This work was supported by the National Natural Science Foundation of China under grant nos. 51177140 and 61371033.

REFERENCES

[1] C. W. Deisch, “Switching control method changes power converter into a current source,” *in Proc. IEEE Power Electron. Sepc. Conf.*, pp. 300-306, 1978.

[2] R. Redl and N. O. Sokal, “Current-mode control, five different types, used with the three basic classes of power converters: small-signal ac and large-signal dc characterization, stability requirements, and implementation of practical circuits,” *in Proc. IEEE Power Electron. Spec. Conf.*, pp. 771-785, 1985.

[3] Texas Instruments, LM3409 datasheet. http://www.ti.com/lit/ds/symlink/lm3409.pdf, 2016.

[4] Linear Technology, LTC3869 datasheet. http://cds.linear.com/docs/en/datasheet/38692fb.pdf, 2011.

[5] Analog Devices, ADP1882 datasheet. http://www.analog.com/media/en/technical-documentation/data-sheets/ADP1882_1883.pdf, 2010.

[6] Maxim, MAX17512 datasheet. https: //datasheets.maximintegrated.com/en/ds/MAX17512.pdf, 2011.

[7] C. P. Basso, “Switch-mode power supplies: SPICE simulations and practical designs,” 2nd ed., New York, NY, USA: McGraw-Hill, 2015, pp. 258-262.

[8] J. Sun, “Small-signal modeling of variable-frequency pulsewidth modulators,” *IEEE Tran. Aerosp. Electron. Syst.*, Vol. 38, No. 3, pp. 1104-1108, Jul. 2002.

[9] R. Redl and I. Novak, “Instability in current-mode controlled switching voltage regulators,” *in Proc. IEEE Power Electron. Spec. Conf.*, pp. 17-28, 1981.

[10] D. J. Packard, “Discrete modeling and analysis of switching regulators,” Ph. D. dissertation, California Institute Technology, CA, May, 1976.

[11] A. R. Brown and R. D. Middlebrook, “Sampled-data modeling of switched regulators,” *in Proc. IEEE Power Electron. Spec. Conf.*, pp. 349-369, 1981.

[12] R. B. Ridley, “A new, continuous-time model for current-mode control,” *IEEE Trans. Power Electron.*, Vol. 6, No. 2, pp. 271-280, Apr. 1991.

[13] W. H. Ki, “Analysis of subharmonic oscillation of fixed-frequency current-programming switch mode power converters,” *IEEE Trans. Circuits Syst. I, Fundam. Theory and Appl.*, Vol. 45, No. 1, pp. 104-108, Jan. 1998.

[14] C. K. Tse and Y. M. Lai, "Controlling bifurcations in power electronics: a conventional practice re-visited," *Latin American Applied Research*, Vol. 31, pp. 177-184, 2001.

[15] J. H. B. Deane, “Chaos in a current-mode controlled boost dc-dc converter,” *IEEE Trans. Circuits Syst. I, Fundamental Theory and Applications*, Vol. 39, No. 8, pp. 680-683, Aug. 1992.

[16] C. K. Tse, S. C. Fung, and M. W. Kwan, “Experimental confirmation of chaos in a current-programmed Ćuk converter,” *IEEE Trans. Circuits Syst. I, Fundam. Theory and Appl.*, Vol. 43, No. 7, pp. 605-608, Jul. 1996.

[17] Y. F. Chen, C. K. Tse, S. S. Qiu, L. Lindenmüller, and W. Schwarz, “Coexisting fast-scale and slow-scale instability in current-mode controlled DC/DC converters: analysis,

simulation and experimental results," *IEEE Trans. Circuits Syst. I, Reg. Papers*, Vol. 55, No. 10, pp. 3335-3348, Nov. 2008.

[18] G. H. Zhou, B. C. Bao, J. P. Xu, "Complex dynamics and fast-slow scale instability in current-mode controlled buck converter with constant current load," *Int. J. Bifurc. Chaos*, Vol. 23, No. 4, pp. 1350062, Apr. 2013.

[19] S. Banerjee, S. Parui, and A. Gupta, "Dynamical effects of missed switching in current-mode controlled dc-dc converters," *IEEE Trans. Circuits Syst. II*, *Express Briefs*, Vol. 51, No. 12, pp. 649-654, Dec. 2004.

[20] G. H. Zhou, J. P. Xu, and B. C. Bao, "Symmetrical dynamics of current- mode controlled switching dc-dc converters," *Int. J. Bifurc. Chaos*, Vol. 22, No. 1, pp. 1250008, Jan. 2012.

[21] B. C. Bao, G. H. Zhou, J. P. Xu, and Z. Liu, "Unified classification of operation state regions for switching converters with ramp compensation," *IEEE Trans. Power Electron.*, Vol. 26, No. 7, pp. 1968-1975, Jul. 2011.

[22] C. C. Fang, "Asymmetric instability conditions for peak and valley current programmed converters at light loading," *IEEE Trans. Circuits Syst. I, Reg. Papers*, Vol. 61, No. 3, pp. 922-929, Mar. 2014.

[23] A. E. Aroudi, J. Calvente, R. Giral, M. Al-Numay, and L. Martínez-Salamero, "Boundaries of subharmonic oscillations associated to filtering effects of controllers and current sensors in switched converters under CMC," *IEEE Trans. Ind. Electron.*, Vol. 63, No. 8, pp. 4826-4837, Aug. 2016.

[24] G. H. Zhou, J. P. Xu, and J. P. Wang, "Constant-frequency peak-ripple-based control of buck converter in CCM: review, unification, and duality," *IEEE Trans. Ind. Electron.*, Vol. 61, No. 3, pp. 1280-1291, Mar. 2014.

[25] C. C. Fang and R. Redl, "Subharmonic instability limits for the peak-current-controlled buck converter with closed voltage feedback loop," *IEEE Trans. Power Electron.*, Vol. 30, No. 2, pp. 1085-1092, Feb. 2015.

[26] C. C. Fang and R. Redl, "Subharmonic instability limits for the peak-current-controlled boost, buck-boost, flyback, and SEPIC converters with closed voltage feedback loop," *IEEE Trans. Power Electron.*, 2016, DOI: 10.1109/TPEL.2016.2587827.

[27] J. Li and F. C. Lee, "New modeling approach and equivalent circuit representation for current-mode control," *IEEE Trans. Power Electron.*, Vol. 25, No. 5, pp. 1218-1230, May 2010.

[28] C. C. Fang, "Closed-form critical conditions of instabilities for constant on-time controlled buck converters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, Vol. 59, No. 12, pp. 3090-3097, Dec. 2012.

[29] X. M. Duan and A. Q. Huang, "Current-mode variable-frequency control architecture for high-current low-voltage DC-DC converters," *IEEE Trans. Power Electron.*, Vol. 21, No. 4, pp. 1133-1137, Jul. 2006.

[30] Y. Y. Yan, F. C. Lee, and P. Mattavelli, "Unified three-terminal switch model for current mode controls," *IEEE Trans. Power Electron.*, Vol. 27, No. 9, pp. 4060-4070, Sep. 2012.

[31] S. L. Tian, F. C. Lee, J. Li, Q. Li, and P. H. Liu, "Three-terminal switch model of constant on-time current mode with external ramp compensation," *IEEE Trans. Power Electron.*, Vol. 31, No. 10, pp. 7311-7319, May 2016.

[32] J. Cortés, V. Šviković, P. Alou, J. A. Oliver, J. A. Cobos, and R. Wisniewski. "Accurate analysis of subharmonic oscillations of V^2 and V^2I_c controls applied to buck converter," *IEEE Trans. Power Electron.*, Vol. 30, No. 2, pp. 1005-1018, Feb. 2015.

[33] J. P. Wang, B. C. Bao, J. P. Xu, G. H. Zhou, and W. Hu, "Dynamical effects of equivalent series resistance of output capacitor in constant on-time controlled buck converter," *IEEE Trans. Ind. Electron.*, Vol. 60, No. 5, pp. 1759-1768, May 2013.

[34] X. Zhang, J. P. Xu, B. C. Bao, and G. H. Zhou, "Asynchronous-switching map based stability effects of circuit parameters in fixed off-time controlled buck converter," *IEEE Trans. Power Electron*., Vol. 31, No. 9, pp. 6686-6697, Sep. 2016.

[35] J. P. Wang, J. P. Xu, and B. C. Bao, "Analysis of pulse bursting phenomenon in constant on-time-controlled buck converter," *IEEE Trans. Ind. Electron.*, Vol. 58, No. 12, pp. 5406-5410, Dec. 2011.

[36] C. C. Fang, "Critical conditions for a class of switched linear systems based on harmonic balance: applications to DC-DC converters," Nonlinear Dynamics, Vol. 70, No. 3, pp. 1767-1789, Nov. 2012

Xi Zhang was born in Jiangsu, China. He received his B.S. degree in Electronic Science and Technology from the Changshu Institute of Technology, Suzhou, China, in 2010; and his M.S. degree in Computer Application Technology from Changzhou University, Changzhou, China, in 2013. He is presently working towards his Ph.D. degree in Electrical Engineering in the School of Electrical Engineering, Southwest Jiaotong University, Chengdu, China. His current research interests include the control techniques and dynamic modeling of switching power converters.

Jianping Xu received his B.S. and Ph.D. degrees in Electronic Engineering from the University of Electronics Science and Technology of China, Chengdu, China, in 1984 and 1989, respectively. Since 1989, he has been with the School of Electrical Engineering, Southwest Jiaotong University, Chengdu, China, where he has been a Professor since 1995. From November 1991 to February 1993, he was with the Department of Electrical Engineering, University of Federal Defense Munich, Munich, Germany, as a Visiting Research Fellow. From February 1993 to July 1994, he was with the Department of Electrical Engineering and Computer Science, University of Illinois at Chicago, Chicago, IL, USA, as a Visiting Scholar. His current research interests include the modeling, analysis, and control of power electronic systems.

Jiahui Wu was born in Huanggang, China. He received his B.S. degree in Electronics Engineering from the Xi'an University of Technology, Xi'an, China, in 2015. He is presently working towards his M.S. degree in Electrical Engineering from Southwest Jiaotong University, Chengdu, China. His current research interests include DC-DC converters, AC motor control, and PWM converter/inverter systems.

Bocheng Bao received his B.S. and M.S. degrees in Electronic Engineering from the University of Electronics Science and Technology of China, Chengdu, China, in 1986 and 1989, respectively; and his Ph.D. degree from the Department of Electronic Engineering, Nanjing University of Science and Technology, Nanjing, China, in 2010. Dr. Bao has spent more than 19 years working in the industry, and he has served as a Senior Engineer and as a General Manager in several enterprises. From June 2008 to January 2011, he was a Professor in the School of Electrical and Information Engineering, Jiangsu University of Technology, Changzhou, China. Since March 2011, he has been a Professor in the School of Information Science and Engineering, Changzhou University, Changzhou, China. From June 2013 to December 2013, he was with the Department of Electrical and Computer Engineering, University of Calgary, Calgary, AB, Canada, as a Visiting Scholar. His current research interests include the analysis and simulation of bifurcation and chaos in power electronic circuits, and nonlinear circuits and systems.

Guohua Zhou received his B.S. degree in Electronics and Information Engineering and his M.S. and Ph.D. degrees in Electrical Engineering from Southwest Jiaotong University, Chengdu, China, in 2005, 2008 and 2011, respectively. He is presently working as a Professor in the School of Electrical Engineering, Southwest Jiaotong University. From March 2010 to September 2010, he was a Research Assistant in the Department of Electronic and Information Engineering, Hong Kong Polytechnic University, Kowloon, Hong Kong. From October 2010 to March 2011, he was a Visiting Scholar (and a Joint Ph.D. Student) in the Center for Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg, VA, USA. His current research interests include the modulation and control of power electronics systems, the dynamical modeling and analysis of switching power converters, and renewable energy applications of power electronics.

Kaitun Zhang was born in Fuyang, China. He received his B.S. and M.S. degrees in Electronics Engineering from Southwest Jiaotong University, Chengdu, China, in 2014 and 2017, respectively. He is presently working as a Product Testing Engineer at SunGrow Company, Hefei, China. His current research interests include DC-DC converters, dynamic modeling, stability analysis, and PWM converter/inverter systems.