

# A Novel Switched-Capacitor Based High Step-Up dc/dc Converter for Renewable Energy System Applications

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## Abstract

This paper presents a new high step-up dc/dc converter for renewable energy systems in which a high voltage gain is provided by using a coupled inductor. The operation of the proposed converter is based on a charging capacitor with a single power switch in its structure. A passive clamp circuit composed of capacitors and diodes is employed in the proposed converter for lowering the voltage stress on the power switch as well as increasing the voltage gain of the converter. Since the voltage stress is low in the provided topology, a switch with a small ON-state resistance can be used. As a result, the losses are decreased and the efficiency is increased. The operating principle and steady-states analyses are discussed in detail. To confirm the viability and accurate performance of the proposed high step-up dc-dc converter, several simulation and experimental results obtained through PSCAD/EMTDC software and a built prototype are provided.

**Key words:** High gain DC-DC converters, switched-capacitor, renewable energy systems, Coupled inductor

## I. INTRODUCTION

In order to save the natural environment of the earth, the development of clean pollution free energy has had a major role in the last decade [1]. For dealing with the issue of global warming, clean energies, such as fuel cells (FC), photovoltaic (PV) sources, wind energy, etc., have been rapidly promoted [2-3]. Generally, the maximum power point (MPP) voltage of a typical PV panel is in the range of 15-40 V depending on the power capacity of the PV panel [4-7]. Thus, a high voltage gain converter is required to obtain a high output voltage from a low input voltage, especially in grid connected applications [8-9]. Conventional boost and buck-boost converters can be used to provide a high output voltage. However, they must work with an extremely high duty cycle. This is limited due to a number of issues such as the impact of the power switches, the diodes, and the equivalent series resistances (ESR) of the inductors and capacitors. Moreover, its control and stability at high duty cycles is very complex [10-11]. One solution is utilizing flyback converters.

However, the transformers used in this kind of converter increase the cost, the size and the voltage stress on main switch, and the leakage losses become large [12]. The use of active-clamps [13-14] and resistor-capacitor-diodes (RCD) [15] can largely eliminate these problems, but they are not very economic due to the high power switch driver circuits [16]. In high-voltage transformers with a very high turns ratio, the characteristics of non-ideal elements are getting worse and worse. Therefore, the leakage inductance of the transformer results in an adverse voltage spike. As a result, the circuit elements experience failure [17]. In addition, the distribution capacitors of the transformers cause current spikes. Both of these non-ideal features increase the switching losses and decrease the efficiency of the converter [18]. Several converters with a high voltage gain have been proposed in [19-26]. Coupled inductors are used to get a high voltage gain in non-isolated converters [19-21]. The main problem with these kinds of converters is the leakage inductance of the coupled inductor, which increases the voltage stress on the main switch [22]. Active-clamp circuits are used to eliminate these so-called problems. In [23-24], the switching capacitor techniques has been suggested to achieve a high step-up voltage gain. However, it should be noted that, in these cases, the switch must withstand a high current which decreases the efficiency of the converter. A

conventional boost converter in combination with a switched-capacitor converter has been presented in [25]. However, the rating of the switching components limits the output voltage. For high voltage applications, a new structure has been presented in [26]. However, it produces negative voltage at the output.

## II. OPERATING PRINCIPLES OF THE PROPOSED CONVERTER

Fig. 1 shows the circuit configuration of the proposed converter. The proposed converter is composed of a coupled inductor, a switch, diodes and capacitors. The diodes  $D_1$  and  $D_2$  are clamp diodes, and the capacitors  $C_1$  and  $C_2$  are the clamp capacitors of the clamp circuit of the proposed converter. The energy of the leakage inductor of the primary winding ( $N_1$ ) through the diodes  $D_1$  and  $D_2$  is stored in the capacitors  $C_1$  and  $C_2$ . In the proposed converter, the capacitors are charged in parallel and discharged in series to increase the output voltage gain. Generally, the leakage inductance of the coupled inductor has the ability to increase the voltage stress on the switches. However, in the proposed converter a passive-clamp circuit is used to eliminate this problem.

The features of the proposed structure are as follows. 1) The energy of the leakage inductors of the coupled inductor is recycled. This feature reduces the losses and prevents voltage spikes on the main switch. 2) A high voltage gain is provided by using a coupled inductor and capacitor charging techniques. 3) The voltage stress on the main switch is very low. Thus, a switch with a low voltage rating and a low ON-state resistance ( $R_{DS-ON}$ ) can be used. 4) The main switch is placed in series with the source. Therefore, it can control the energy flow from the source to the load.

To simplify the analysis of the proposed converter, the following assumptions are considered:

- All of the components are ideal. The ON-state resistance ( $R_{DS-ON}$ ) of the switch, the forward voltage drop of the diodes, and the ESR of the coupled inductor and capacitors are ignored.
- The turns ratio  $n$  of the coupled inductor is equal to  $N_2 / N_1$ .
- The capacitors  $C$ ,  $C_1$ ,  $\dots$ ,  $C_4$ , and  $C_o$  are large enough. As a result, so the voltages across them are considered constant during one switching period.

The operating principles in the CCM are presented in detail.

### A. CCM Operation

In the CCM, the proposed converter has five operating modes. A simplified circuit model of the proposed converter in different operating modes is shown in Fig. 2. The coupled inductor is modeled as a magnetizing inductor  $L_m$ , a primary

leakage inductor  $L_{K1}$ , a secondary leakage inductor  $L_{K2}$ , and an ideal transformer.

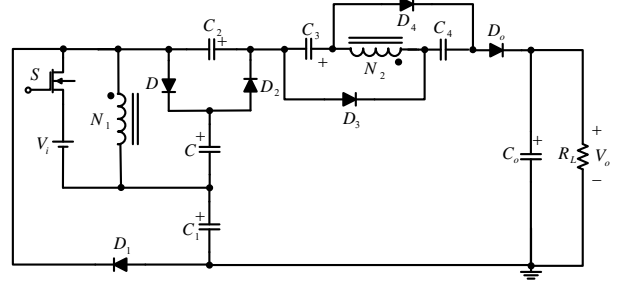


Fig. 1. Circuit configuration of the proposed converter.

### Mode I ( $0 < t < t_1$ )

As shown in Fig. 2(a), the switch  $S$  and the diodes  $D$ ,  $D_3$  and  $D_4$  are turned on. The dc-source energy is across  $L_{K1}$ ,  $L_m$  and  $S$ . The capacitor  $C$  is charged through the diode  $D$ . The magnetizing current  $i_{Lm}$  is decreasing because the energy of the magnetizing inductor  $L_m$  is discharging into the secondary winding and the energy is reduced by charging the capacitors  $C_3$  and  $C_4$ . Thus, the currents  $i_{D3}$  and  $i_{D4}$  are decreasing. The current  $i_{LK2}$  is also decreasing according to  $i_{Lm} / n$ . The output load is supplied through the energy stored in  $C_o$ . The first mode ends when the current  $i_{LK1}$  is equal to  $i_{Lm}$  at  $t = t_1$ . For this mode the following equations are true:

$$\frac{di_{Lm}^I(t)}{dt} = \frac{v_{Lm}}{L_m} \quad (1)$$

$$\frac{di_{LK1}^I(t)}{dt} = \frac{V_i - v_{Lm}}{L_{K1}} \quad (2)$$

$$i_{LK2}^I(t) = \frac{i_{Lm}^I(t) - i_{LK1}^I(t)}{n} \quad (3)$$

$$V_C = V_i \quad (4)$$

Where,  $n$ ,  $v_{Lm}$ ,  $i_{Lm}^I$ ,  $i_{LK1}^I$  and  $i_{LK2}^I$  are the turns ratio of the coupled inductor  $T_1$ , the magnetizing inductor voltage, the magnetizing inductor current, and the primary and secondary leakage inductor currents in mode I, respectively.

### Mode II ( $t_1 \leq t < t_2$ )

During this operating mode, the switch  $S$  and the diodes  $D$  and  $D_o$  are turned on. The input voltage source  $V_i$  is in series with the capacitors  $C_1$ ,  $C_2$ ,  $\dots$ ,  $C_4$  and the secondary winding  $N_2$ . Thus, they supply the output capacitor  $C_o$  and the load  $R_L$ .

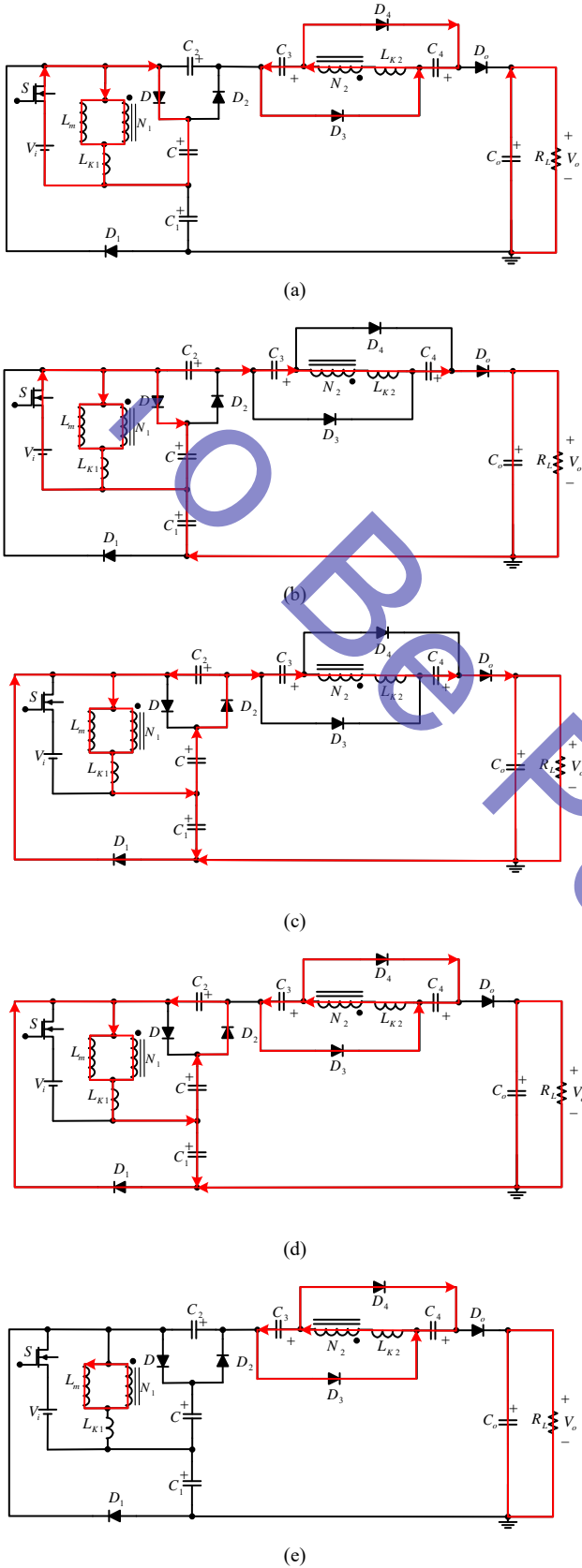


Fig. 2. Equivalent circuits of different operating modes during one switching period at the CCM: (a) Mode I; (b) Mode II; (c) Mode III; (d) Mode IV; (e) Mode V.

Meanwhile, the capacitor  $C$ , the magnetizing inductor  $L_m$ , and the primary leakage inductor  $L_{K1}$  also receive energy from the source  $V_i$ . Thus, the currents  $i_{Lm}$ ,  $i_{LK1}$  and  $i_{D5}$  increase. The switch  $S$  is turned off at the end of this operating mode ( $t = t_2$ ). The following equations can be written during this operating mode:

$$i_{Lm}^{II}(t) = i_{LK1}^{II}(t) - ni_{LK2}^{II}(t) \quad (5)$$

$$i_{D5}^{II}(t) = i_{D5}^{II}(t) = i_{Lm}^{II}(t) + (1+n)i_{LK2}^{II}(t) + i_C^{II}(t) \quad (6)$$

$$\frac{di_{LK2}^{II}(t)}{dt} = \frac{di_{D5}^{II}}{dt} = \frac{nv_{Lm} + V_{C1} + V_{C2} + V_{C3} + V_{C4} + V_i - V_o}{L_{K2}} \quad (7)$$

Where,  $i_{D5}^{II}$ ,  $v_{N2}$ ,  $V_o$ ,  $V_{C1}$ ,  $V_{C2}$ ,  $V_{C3}$  and  $V_{C4}$  are the current of the diode  $D_5$ , the secondary winding voltage, the output voltage, the capacitors  $C_1$ ,  $C_2$ ,  $\dots$ ,  $C_4$  and the voltage in second mode, respectively.

**Mode III** ( $t_2 \leq t < t_3$ )

During this period, while the switch  $S$  is turned off, the secondary leakage inductance  $L_{K2}$  continues charging the capacitor  $C_o$ . Meanwhile, the energy stored in the primary leakage inductance  $L_{K1}$  and the capacitor  $C$  is discharged into the capacitor  $C_2$  through the diode  $D_2$ . Additionally, through the diode  $D_1$ , the energy stored in the primary leakage inductance is discharged into the capacitor  $C_1$ . At the same time,  $L_{K2}$  maintains the previous mode current and in series with the capacitors  $C_2$ ,  $C_3$ , and  $C_4$  supplies the output capacitor  $C_o$  and the load  $R_L$ . The currents  $i_{LK1}$  and  $i_{LK2}$  are rapidly decreased through discharging into the capacitors  $C_1/C_2$  and  $C_o$ , respectively. However, the current  $i_{Lm}$  is increased because  $L_m$  receives energy from  $L_{K2}$ . This mode ends when the current  $i_{LK2}$  becomes zero. In this mode, the following equations are valid:

$$i_{Lm}^{III}(t) = i_{LK1}^{III}(t) - ni_{LK2}^{III}(t) \quad (8)$$

$$\frac{di_{LK1}^{III}(t)}{dt} = \frac{-V_{C1} - v_{Lm}}{L_{K1}} \quad (9)$$

$$\frac{di_{LK1}^{III}(t)}{dt} = \frac{-V_{C2} + V_C - v_{Lm}}{L_{K1}} \quad (10)$$

$$i_{LK1}^{III}(t) = i_{D1}^{III}(t) + i_{D2}^{III}(t) \quad (11)$$

$$\frac{di_{LK2}^{III}(t)}{dt} = \frac{nv_{Lm} + V_{C2} + V_{C3} + V_{C4} - V_o}{L_{K2}} \quad (12)$$

By using (9) and (10), the following equation can be extracted:

$$V_{C2} = V_{C1} + V_C \quad (13)$$

#### Mode IV ( $t_3 \leq t < t_4$ )

During this period, the diodes  $D_1$ ,  $D_2$ ,  $D_3$  and  $D_4$  are turned on. The energy stored in  $L_m$  is discharged into the capacitors  $C_1$ ,  $C_3$  and  $C_4$ . The energy stored in the capacitor  $C$  and the energy stored in  $L_m$  charge the capacitor  $C_2$ . The currents  $i_{LK1}$ ,  $i_{D1}$  and  $i_{D2}$  are decreased because  $L_{K1}$  releases its energy into the capacitors  $C_1$  and  $C_2$  through the diodes  $D_1$  and  $D_2$ . The energy stored in the capacitor  $C_o$  is discharged to the load  $R_L$ . This mode ends when the current  $i_{LK1}$  becomes zero. For this mode the following equations are obtained:

$$\frac{di_{LK2}^{IV}(t)}{dt} = 2 \frac{di_{D3}^{IV}(t)}{dt} = \frac{nv_{Lm} + V_{C3}}{L_{K2}} \quad (14)$$

$$\frac{di_{LK2}^{IV}(t)}{dt} = 2 \frac{di_{D4}^{IV}(t)}{dt} = \frac{nv_{Lm} + V_{C4}}{L_{K2}} \quad (15)$$

By using (14) and (15), the following equation can be extracted:

$$V_{C3} = V_{C4} \quad (16)$$

As can be seen from (16), the capacitors  $C_3$  and  $C_4$  have the same voltages amplitudes. As a result, their capacities should be equal.

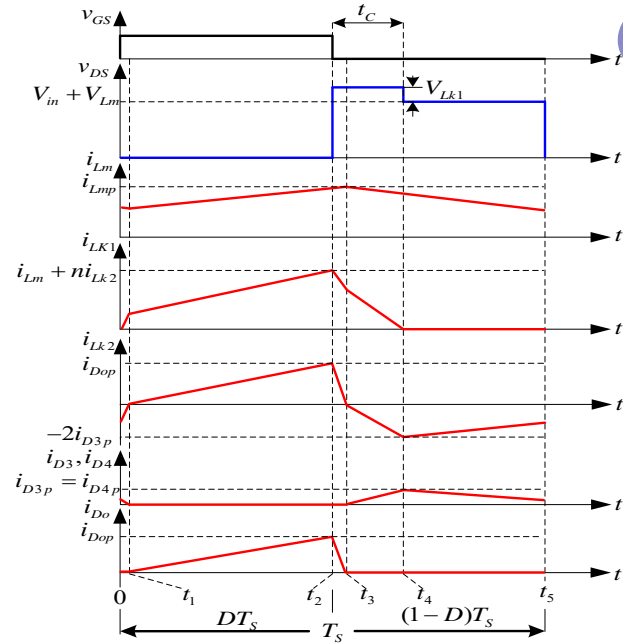


Fig. 3. Key waveforms of the proposed converter in the CCM.

#### Mode V ( $t_4 \leq t < t_5$ )

During this period,  $L_m$  discharges its energy into the capacitors  $C_3$  and  $C_4$ . The current  $i_{Lm}$  is decreased

because  $L_m$  discharges its energy into the capacitors  $C_3$  and  $C_4$  through the secondary winding and the diodes  $D_3$  and  $D_4$ . The energy stored in the capacitor  $C_o$  is discharging to the load  $R_L$ . This mode ends when the switch  $S_1$  is turned on. The Equations associated with mode V are as follows:

$$\frac{di_{Lm}^V(t)}{dt} = \frac{v_{Lm}}{L_m} \quad (17)$$

$$i_{LK1}^V = 0 \quad (18)$$

$$\frac{di_{LK2}^V(t)}{dt} = 2 \frac{di_{D3}^V(t)}{dt} = 2 \frac{di_{D4}^V(t)}{dt} = \frac{nv_{Lm} + V_{C3}}{L_{K2}} \quad (19)$$

Based on the aforementioned information and equations in the CCM, the key waveforms of the proposed converter in one switching period are shown in Fig. 3.

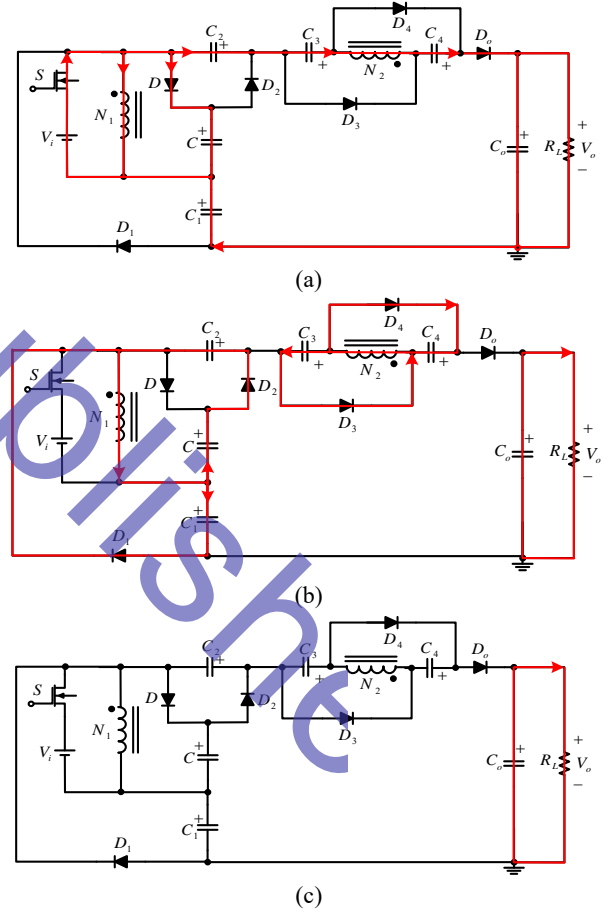


Fig. 4. Equivalent circuits of different operating modes during one switching period in DCM: (a) Mode I; (b) Mode II; (c) Mode III.

#### DCM Operation

In DCM, to simplify the analysis, the primary and secondary inductors ( $L_{K1}$ ,  $L_{K2}$ ) are neglected. Therefore, the proposed converter has three operating modes as shown in Fig. 4.

### Mode I ( $0 < t < t_1$ )

According to Fig. 4(a), the input source  $V_i$  is in series with the capacitors  $C_1, C_2, \dots, C_4$  and the secondary windings and they feed the output capacitor  $C_o$  and the load  $R_L$ . The current  $i_{Lm}$  is increasing because  $L_m$  is receiving energy from the source  $V_i$ . The capacitor  $C$  is paralleled with the source  $V_i$  through the diode  $D$ . This mode ends when the main switch is turned off. The following equations are true for this mode:

$$i_i^I(t) = i_{Lm}^I(t) + ni_{N2}^I(t) + i_C^I(t) \quad (20)$$

$$\frac{di_{Lm}^I(t)}{dt} = \frac{V_i}{L_m} \quad (21)$$

$$V_C = V_i \quad (22)$$

Where,  $i_{N2}^I$  is the secondary winding current in mode I.

### Mode II ( $t_1 \leq t < t_2$ )

During this period, the inductor  $L_m$  releases its energy into the capacitors  $C_1, C_2, \dots, C_4$ . Thus, the currents  $i_{D1}, i_{D2}, \dots, i_{D4}$  are decreasing. The energy saved in the capacitor  $C_o$  is supplying the load  $R_L$ . This mode ends when the current  $i_{Lm}$  becomes zero. For this mode the following equations are true:

$$i_i^{II}(t) = i_{DS}^{II}(t) = 0 \quad (23)$$

$$\frac{di_{Lm}^{II}(t)}{dt} = \frac{-V_{C1}}{L_m} = \frac{-V_{C2} + V_C}{L_m} \quad (24)$$

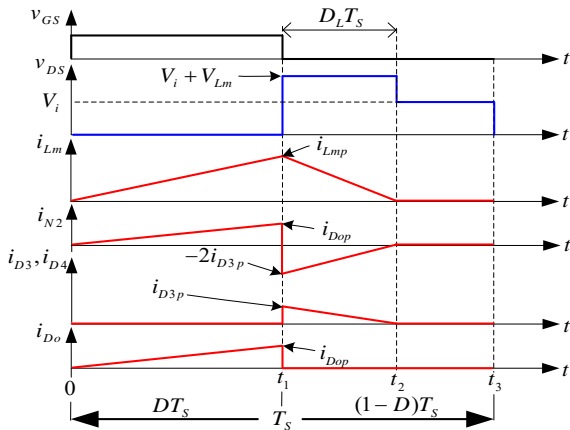


Fig. 5. Key waveforms of the proposed converter in the DCM.

### Mode III ( $t_2 \leq t < t_3$ )

During this period, the switch  $S$  is turned off. Meanwhile,  $L_m$  is completely out of energy and the capacitor  $C_o$  is discharging its energy to the load  $R_L$ . This

mode ends when the switch  $S$  is turned on. For this mode the following equations are extracted:

$$i_i^{III}(t) = i_{DS}^{III}(t) = 0 \quad (25)$$

$$i_{Lm}^{III}(t) = i_{N2}^{III}(t) = 0 \quad (26)$$

Based on the aforementioned information and equations, the key waveforms of the proposed converter are shown in Fig. 5 in during a switching period in the DCM.

## III. STEADY STATE ANALYSIS OF THE PROPOSED CONVERTER

### A. CCM Operation

In this section, the secondary leakage inductance  $L_{K2}$  of the coupled inductor is transferred to its primary side. As a result, the equivalent primary leakage inductance  $L_K$  is equal to the sum of the primary leakage inductance  $L_{K1}$  and it is transferred to the secondary leakage inductance  $L'_{K2}$ . At the CCM, the time durations of modes I and III are very short in compared with a switching period. Thus, only modes II, IV, and V are considered.

Fig. 6 shows the relationship between the clamp capacitors charge and discharge currents of the proposed converter by assuming that the magnetizing current  $i_{Lm}$  is ripple-less. By ignoring modes I and III,  $t_c$  is the fourth time duration mode and  $D_C$  is its corresponding duty cycle. The stored energy in the equivalent primary leakage inductance  $L_K$  at the time interval  $t_c$  is discharged into the clamp capacitors  $C_1$  and  $C_2$ . Since the average capacitor currents  $I_{C1}, I_{C2}, \dots, I_{C5}$  is zero at the steady state, the average values of  $I_{D1}, I_{D2}, \dots, I_{D5}$  are equal to the average value of  $I_o$ . By setting the charge energy equal to the discharge energy, the following relationships can be written:

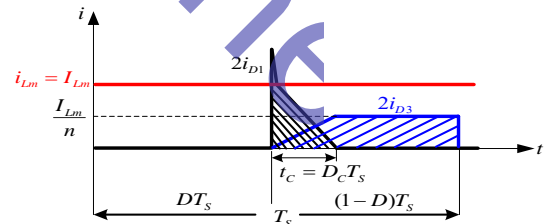


Fig. 6. Relationship between the clamp capacitors charge and discharge currents of the proposed converter.

$$L_K = L_{K1} + L'_{K2} = L_{K1} + n^2 L_{K2} \quad (27)$$

$$I_{D1} = I_{D2} = \dots = I_{D5} = I_o \quad (28)$$

$$\frac{D_C T_s I_{Lm}}{4 T_s} = \frac{I_{Lm} T_s}{4 n T_s} (2 - 2D - D_C) \quad (29)$$

$$D_C = \frac{t_c}{T_s} = \frac{2(1-D)}{1+n} \quad (30)$$

where,  $t_c$  is the time interval shown in Fig. 6.

According to [31], the coupling coefficient of the coupled inductor  $K$  is equal to  $L_m / (L_m + L_K)$ . The following equations can be written based on Fig. 2(b):

$$V_C = V_{in} \quad (31)$$

$$v_{LK}^H = \frac{L_k}{L_m + L_K} V_{in} = (1-K)V_i \quad (32)$$

$$v_{Lm}^H = \frac{L_m}{L_m + L_k} V_i = KV_i \quad (33)$$

$$v_{N2}^H = n v_{Lm}^H = nKV_i \quad (34)$$

$$V_o = V_i + V_{C1} + V_{C2} + V_{C3} + V_{C4} + v_{N2}^H \quad (35)$$

Considering the voltage-second balance principle of the inductance, the following equations can be written:

$$\int_0^{DT_s} v_{LK}^H dt + \int_{DT_s}^{T_s} v_{LK}^{IV} dt = 0 \quad (36)$$

$$\int_0^{DT_s} v_{Lm}^H dt + \int_{DT_s}^{T_s} v_{Lm}^{IV} dt = 0 \quad (37)$$

$$\int_0^{DT_s} v_{N2}^H dt + \int_{DT_s}^{T_s} v_{N2}^{IV} dt = 0 \quad (38)$$

Substituting (27)–(35) into (36)–(38), the voltages  $v_{LK}^{IV}$ ,

$v_{Lm}^{IV}$  and  $v_{N2}^{IV}$  can be derived as follows:

$$V_{LK}^{IV} = \frac{-D(1+n)(1-K)}{2(1-D)} V_i \quad (39)$$

$$V_{Lm}^{IV} = \frac{-DK}{(1-D)} V_i \quad (40)$$

$$V_{N2}^{IV} = \frac{-nDK}{(1-D)} V_i \quad (41)$$

In mode IV, the capacitors  $C_1$ ,  $C_2$ ,  $C_3$  and  $C_4$  are charged. Considering (39)–(41), the voltage across the capacitors  $C_1$ ,  $C_2$ ,  $C_3$  and  $C_4$  are obtained as follows:

$$V_{C1}^{IV} = -V_{Lm}^{IV} - V_{LK}^{IV} = \frac{D}{2} \left[ \frac{(1+K) + n(1-K)}{(1-D)} \right] V_i \quad (42)$$

$$V_{C2}^{IV} = -V_{Lm}^{IV} - V_{LK}^{IV} + V_C = \left[ \frac{3 + D(K-2) + nD(1-K)}{(1-D)} \right] \frac{V_i}{2} \quad (43)$$

$$V_{C3}^{IV} = V_{C4}^{IV} = -V_{N2}^{IV} = \frac{nDK}{(1-D)} V_i \quad (44)$$

Substituting (34), (42), (43) and (44) into (35), the output voltage is obtained as follows:

$$V_o = \frac{2 + D(K-1) + n(K+D)}{(1-D)} V_i \quad (45)$$

From (45), the voltage gain is obtained as:

$$M_{CCM} = \frac{V_o}{V_i} = \frac{I_i}{I_o} = \frac{2 + D(K-1) + n(K+D)}{(1-D)} \quad (46)$$

When  $K = 1$ , the ideal voltage gain of the proposed converter is written as:

$$M_{CCM} = \frac{V_o}{V_i} = \frac{I_i}{I_o} = \frac{n + nD + 2}{1-D} \quad (47)$$

Fig. 7 shows the variation of the voltage gain  $M_{CCM}$  with respect to different duty cycles  $D$  and while considering various turns ratios. Fig. 8 shows the variation of the voltage gain ( $M_{CCM}$ ) versus the duty cycle ( $D$ ) of the proposed converter when compared with the converters in [4], [27], [28], [29] and [30] in CCM operation under  $n = 3$  and  $K = 1$ .

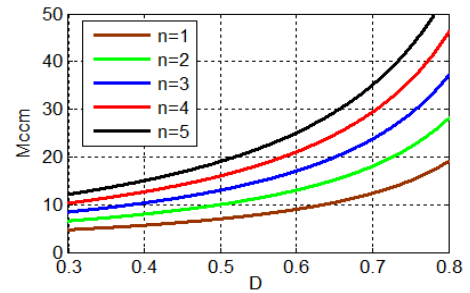


Fig. 7. Voltage gain ( $M_{CCM}$ ) as a function of the duty ratio  $D$  considering various turns ratios.

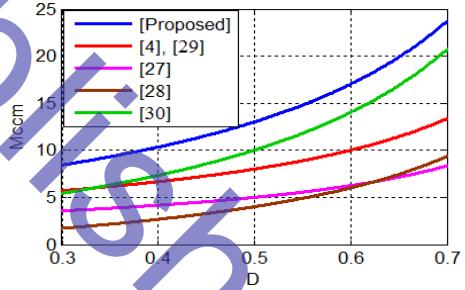


Fig. 8. Voltage gain ( $M_{CCM}$ ) versus the duty cycle ( $D$ ) of the proposed converter when compared with the converters in [4], [24] and [25] in CCM operation under  $n = 3$  and  $K = 1$ .

As can be seen, the proposed converter has the highest voltage gain and it is much larger than the other voltage gain values for all of the duty cycles. According to Table I, at a duty cycle of 0.7 the presented converters in [27] and [28] increase the input voltage up to 8.33 and 9.33, respectively. The presented converters in [4] and [29] can produce 13.33 times the input voltage at the output. The converter presented in [30] produces 20.66 times the input voltage at the output. At the same duty cycle, the proposed converter can increase the voltage gain up to 23.66 at the output. According to the voltage gain of the other converters, the proposed converter

has a salient voltage gain.

TABLE I  
COMPARISON OF THE CONVERTER OUTPUT VOLTAGE GAINS

converter	D		
	D = 0.3	D = 0.5	D = 0.7
[4],[29]	5.71	8	13.33
[27]	3.57	5	8.33
[28]	1.71	4	9.33
[30]	5.42	10	20.66
Proposed	8.42	13	23.66

### B. DCM Operation

In DCM operation, three modes are discussed. Based on Fig. 4(a), the following equations can be formulated:

$$v'_{N2} = nV_i \quad (48)$$

$$V_C = V_i \quad (49)$$

$$V_o = V_i + V_{C1} + V_{C2} + V_{C3} + V_{C4} + v'_{N2} \quad (50)$$

The peak magnetizing inductor current ( $i_{Lmp}$ ) is given as:

$$i_{Lmp} = \frac{DT_s}{L_m} V_i \quad (51)$$

The following equations can be carried out from Fig. 4(b):

$$V_{C1} = -v''_{Lm} \quad (52)$$

$$V_{C2} = -v''_{Lm} + V_C \quad (53)$$

$$V_{C3} = V_{C4} = -v''_{N2} \quad (54)$$

The following equation can be written based on Fig. 4(c):

$$v'''_{Lm} = v'''_{N2} = 0 \quad (55)$$

By applying the voltage-second balance principle of the inductance and by using (48)-(55), the voltage across the capacitors  $C_1, C_2, \dots, C_4$  are achieved as follows:

$$V_{C1} = \frac{D}{D_L} V_i \quad (56)$$

$$V_{C2} = \frac{D_L + D}{D_L} V_i \quad (57)$$

$$V_{C3} = V_{C4} = n \frac{D}{D_L} V_i \quad (58)$$

By substituting (48), (56), (57) and (58) into (50), the output voltage equation is obtained as follows:

$$V_o = \frac{D_L(n+2) + 2D(n+1)}{D_L} V_i \quad (59)$$

From (59), the equation of  $D_L$  is derived as:

$$D_L = \frac{2D(1+n)V_i}{V_o - (n+2)V_i} \quad (60)$$

In addition, the following relationship is always true between the output voltages and currents:

$$V_o = R_L I_o \quad (61)$$

The average values of the diodes  $D_3$  and  $D_4$  currents are given by:

$$I_{D3} = I_{D4} = \frac{I_{Lm} - 2I_{D3}}{2n} \quad (62)$$

By using (62) and knowing that the average current values of the diodes are equal to the average value of  $I_o$ , the peak current of the diodes  $D_3$  and  $D_4$  in the DCM can be obtained as follows:

$$i_{D3p} = i_{D4p} = \frac{i_{Lmp}}{2(n+1)} \quad (63)$$

Based on (37) and Fig. 5, the following equation is true:

$$\frac{1}{2} D_L \frac{i_{Lmp}}{2(n+1)} = I_o \quad (64)$$

Substituting (51), (60) and (61) into (64) yields:

$$\frac{D^2 V_i^2 T_s}{2L_m [V_o - (n+2)V_i]} = \frac{V_o}{R_L} \quad (65)$$

The normalized time constant of the magnetizing inductor ( $\tau_{Lm}$ ) is given by:

$$\tau_{Lm} = \frac{L_m}{R_L T_s} \quad (66)$$

By substituting (56) into (65), the output voltage gain in the DCM ( $M_{DCM}$ ) is obtained as follows:

$$M_{DCM} = \frac{V_o}{V_i} = \frac{n+2}{2} + \sqrt{\left(\frac{n+2}{2}\right)^2 + \frac{D^2}{2\tau_{Lm}}} \quad (67)$$

The curve of the DCM voltage gain versus the duty cycle in different time constants under  $n=3$  is shown in Fig. 9.

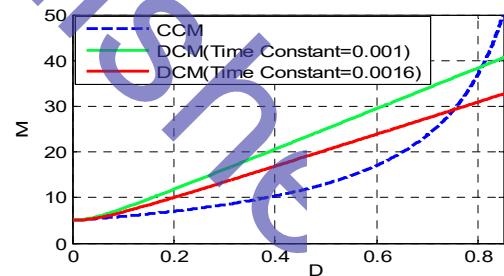


Fig. 9. DCM voltage gain curve versus the duty cycle in different time constants under  $n=3$ .

### C. BCM Operation

BCM is the boundary between the CCM and the DCM. The valley current of the magnetizing inductor at the boundary condition mode is equal to zero. When the proposed converter operates in the BCM, the voltage gains in the CCM and the DCM are equal to each other. Therefore, by getting (47) equal to (67), the boundary normalized time constant of the magnetizing inductor ( $\tau_{LmB}$ ) is achieved as follows:

$$\tau_{LmB} = \frac{L_m f_s}{R_B} = \frac{D(1-D)^2}{4(n+nD+2)(n+1)} \quad (68)$$

The curve variation of  $\tau_{LmB}$  is shown in Fig. 10. When  $\tau_{Lm}$  is larger than  $\tau_{LmB}$ , proposed converter is operating in the CCM; and when  $\tau_{Lm}$  is lower than  $\tau_{LmB}$ , the proposed converter is operating in the DCM.

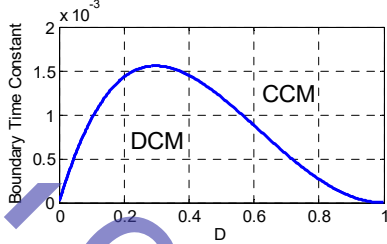


Fig. 10. Boundary condition of the proposed converter for  $n = 3$ .

#### D. Voltage Stress Calculation on the Active Devices

The stresses on the active devices such as the main switch and the diodes are calculated as follows:

$$V_{DS} = V_D = V_{D1} = V_{D2} = \frac{V_i}{1-D} = \frac{V_o}{n+nD+2} \quad (69)$$

$$V_{D5} = V_{D6} = \frac{nV_i}{1-D} = \frac{nV_o}{n+nD+2} \quad (70)$$

$$V_{Do} = \frac{(1+n)V_i}{1-D} = \frac{(1+n)V_o}{n+nD+2} \quad (71)$$

Fig. 11 compares the voltage stress on the main switch of the proposed converter with that of the presented converters in [27], [28] and [29] in CCM operation under  $n = 3$ . As can be seen, the proposed converter has the least voltage in all of the duty cycles.

## IV. VERIFICATION RESULTS

To reconfirm the viability and accurate performance of the proposed high step-up dc-dc converter, some simulation and experimental results through PSCAD/EMTDC software and a built prototype, shown in Fig. 14, based on the detailed specifications compiled in Table II, are presented in this section. Having considered Fig. 1 as the overall configuration of the proposed converter, a utilized dc voltage sources with its magnitude adjusted to 40V has been used in all of the processes for verifying observations, since the output voltage and power of the PV panel is about 15V to 40V and 110W to 290W, respectively [4]. For the same reason, both the simulation and experimental results are shown with 250W of output power.

#### A. Simulation Results

In the simulation platform, the voltage and current waveforms of the proposed converter are shown. Fig. 11 shows the simulation results of the proposed converter with

an output power of 250W. As can be seen and based on Fig. 3, the proposed converter is operating in the CCM. According to the waveform of  $V_{DS}$ , the voltage stress on the switch  $S_1$  is clamped to  $V_{DS} = 80V$ .

Thus, it is possible to use a switch with a low voltage rate and a low ON-state resistance to reduce the losses in the proposed converter. In Figs. 11(b) and 11(d), the waveforms of  $i_{LK1}$  and  $i_{LK2}$  are shown. The second half of the waveform  $i_{LK2}$  charges the capacitors  $C_3$  and  $C_4$  in parallel through the diodes  $D_3$  and  $D_4$ . This verifies the technique used in proposed converter. The waveforms in Figs. 11(c) and 11(e) show that the turn ratio of the coupled inductor used in the proposed converter is equal to 3. Finally, as shown in Fig. 11(f), the output voltage waveform ends up at about 520V, which follows equation (47).

There is a tendency to eliminate electrolytic capacitors in power electronics, since they have a relatively low reliability and a short lifetime. Since the switching frequency of the proposed converter is quite high, the capacitances of  $C_1$ ,  $C_2$ , ...,  $C_4$  used in the proposed converter, do not need to be high. Thus, the FILM capacitors, which are used in LED drivers, can be used in the proposed converter.

#### B. Experimental Results

Experimental waveforms of the proposed converter, such as the input current, the primary and secondary leakage inductors currents, and the diodes  $D_1$  and  $D_2$  currents are shown in Fig. 13 to evaluate the general condition of the proposed topology. It can be seen that all of the voltage and current waveforms are of acceptable quality. These figures show the validity of the steady state analyses.

Symbol	Quantity	Magnitude (Unit)
$f_s$	switching frequency	20kHz
$D$	duty cycle	50%
$V_o$	output voltage	520V
$P_o$	output power	250W
$L_m$	magnetizing inductor	0.1mH
$L_k$	leakage inductor	1.66 $\mu$ H
$C$	capacitor	220 $\mu$ F
$C_1, C_2$	clamp circuit capacitor	47 $\mu$ F
$C_3, C_4$	parallel charged capacitors	22 $\mu$ F
$C_o$	output capacitors	220 $\mu$ F
$n$	turn ratio	3



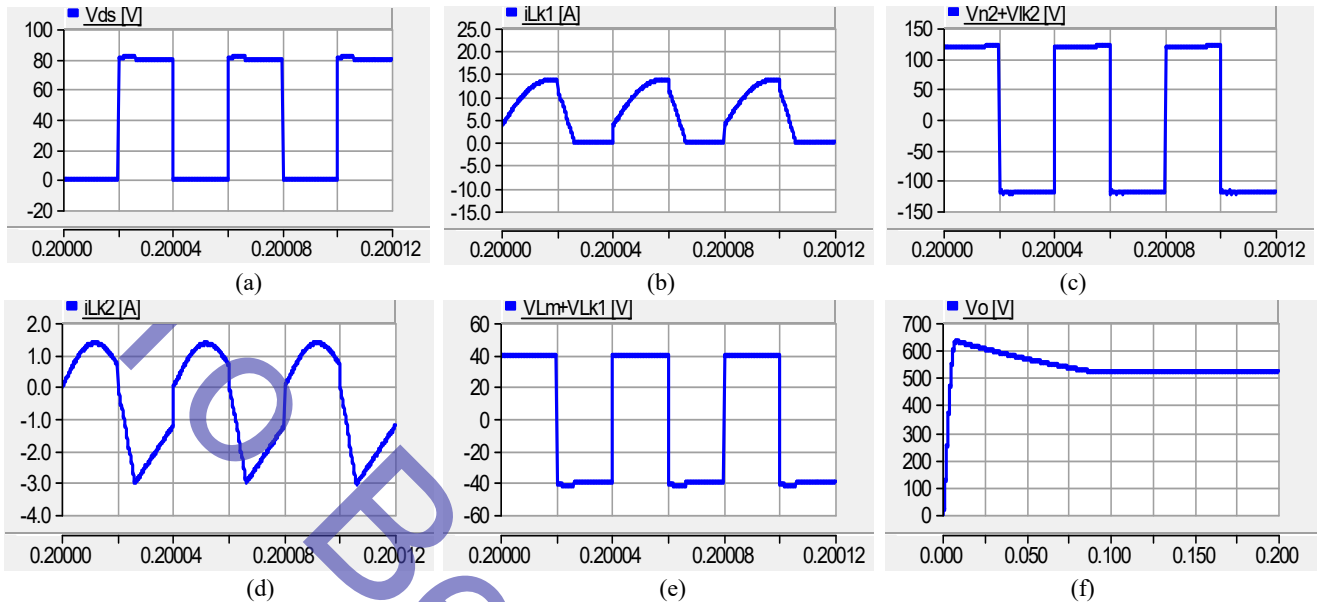


Fig. 11. Simulation results of the proposed converter with output power of 250W .

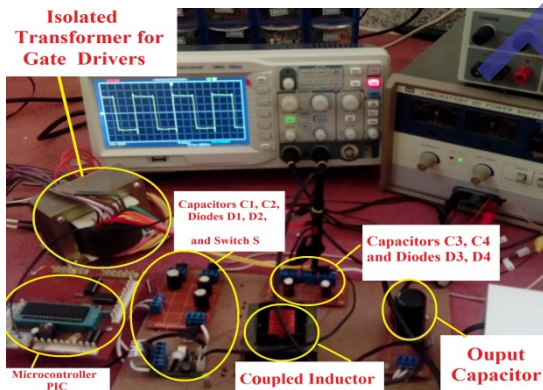


Fig. 12. Experimental prototype of the proposed converter.

In Fig. 13(b), the primary leakage inductor current waveform is shown. In Figs. 13(b), 13(e) and 13(g), the primary winding current waveform and the waveforms of  $i_{D1}$  and  $i_{D2}$  show that the capacitors  $C_1$  and  $C_2$  are charged in parallel. In addition, the secondary winding current waveform and the waveforms of  $i_{D3}$  and  $i_{D4}$ , shown in Figs. 13(d) and 13(h), verify that the capacitors  $C_3$  and  $C_4$  are charged in parallel.

All of the charged capacitors are discharged in series, which verifies the technique that is used in proposed converter. The waveforms in Figs. 13(c) and 13(f) show that the turn ratio of the coupled inductor used in the proposed converter is equal to 3. Finally, as shown in Fig. 13(i), the

output voltage is about 520V, which proves that a high voltage gain is achieved by the proposed converter. The correctness of (47) is also verified by this figure.

Variations in the experimental efficiency of the proposed converter and the converters presented in [27], [29], [32] and [33] for different output powers are shown in Fig. 14. The converter operates at nominal power with an efficiency of about 95.2%.

## V. CONCLUSION

In this paper, a new structure for a high step-up dc/dc boost converter was proposed. In the proposed structure, high voltage gains with low duty cycles are achieved by using capacitors charging techniques and various turn ratios. A comparative study with other similar converters highlights the merits of the proposed topology. In the proposed converter, to eliminate voltage spikes on the main switch, a passive voltage clamp circuit is used. Due to the low voltage stress, low ON-state resistance devices can be used, which increases the efficiency. By recycling the energy of the leakage inductances, the losses are reduced and the efficiency is increased. To confirm the correct performance of the proposed converter, several simulation and experimental results have been presented.

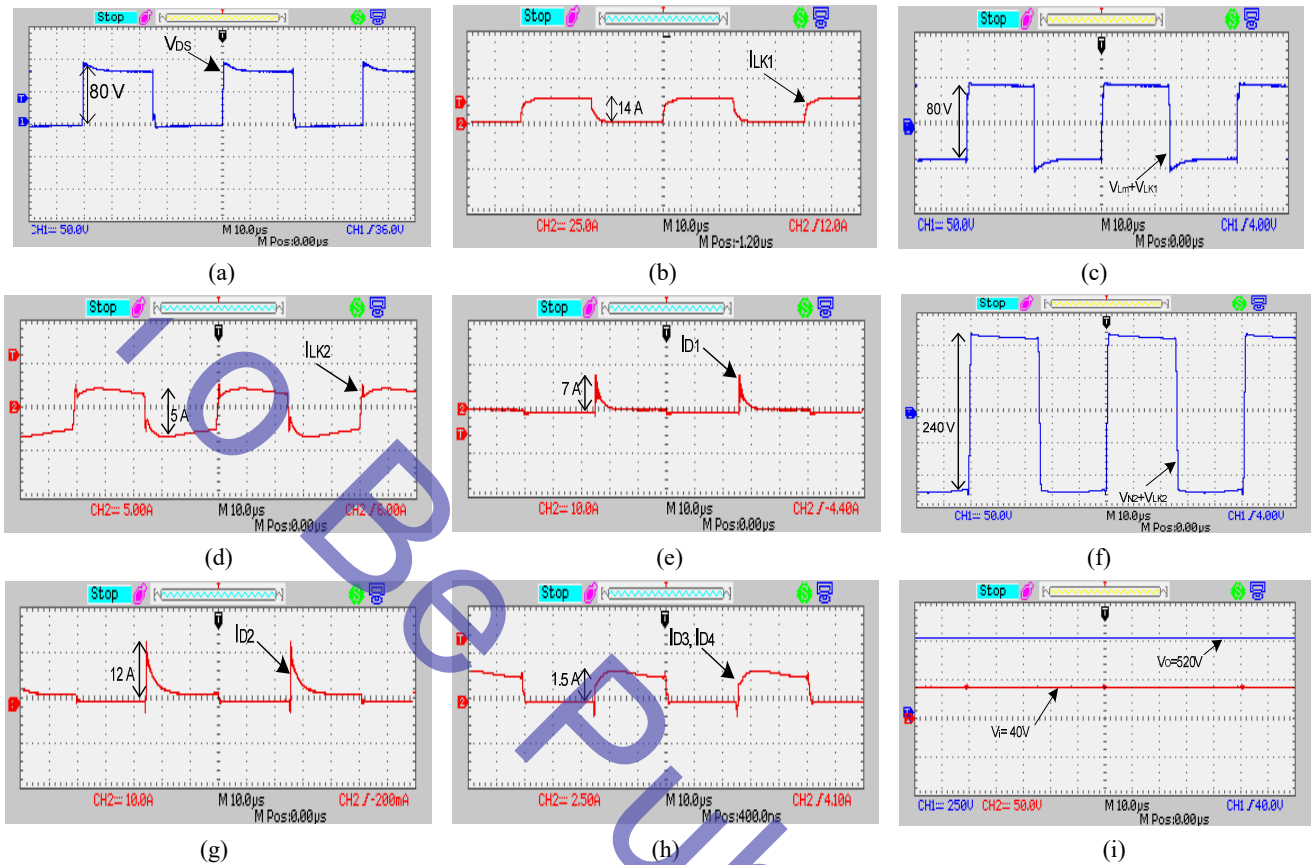


Fig. 13. Experimental results of the proposed converter with output power of 250W .

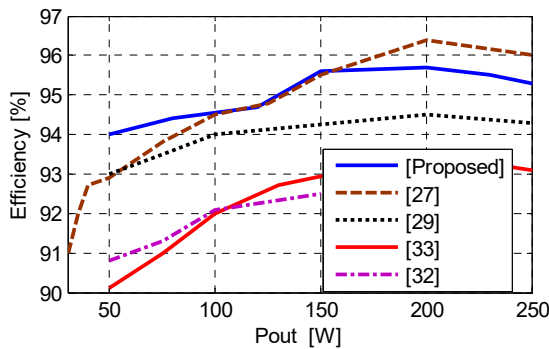


Fig. 14. Measured efficiency of the proposed converter in comparison with the converters presented in [27], [29], [32] and [33].

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