$$i_s(t) = i_s(t_0)\cos[\omega_o(t-t_0)] + \frac{[(V_{in}-V_{cb})/n - V_o] - v_{cr}(t_0)}{Z_o}\sin[\omega_o(t-t_0)] \quad (5)$$

$$v_{cr}(t) = [(V_{in}-V_{cb})/n - V_o] + Z_o i_s(t_0)\sin[\omega_o(t-t_0)] - [(V_{in}-V_{cb})/n - V_o - v_{cr}(t_0)]\cos[\omega_o(t-t_0)] \quad (6)$$

Where, $\omega_o=1/\sqrt{(L_{r2}+L_o)C_r}$, $Z_o=\sqrt{(L_{r2}+L_o)/C_r}$. The switching frequency $f_s(f_s=\omega_s/2\pi)$ is much larger than the frequency $f_o(f_o=\omega_o/2\pi)$, which is composed of the output inductor L_o and the resonant capacitor C_r. Thus, $\omega_o(t-t_0)= \omega_s(t-t_0)\cdot f_o/f_s\approx 0$. Then $\cos[\omega_o(t-t_0)]\approx 1$ and $\sin[\omega_o(t-t_0)]\approx\omega_o(t-t_0)$. Thus, equation (5) and (6) can be simplified as:

$$i_s(t) = i_{Lo}(t) = i_s(t_0) + \frac{[(V_{in}-V_{cb})/n - V_o] - v_{cr}(t_0)}{L_o}(t-t_0) \quad (7)$$

$$v_{cr}(t) = v_{cr}(t_0) + \frac{i_s(t_0)}{C_r}(t-t_0) \quad (8)$$

Mode 2 **[$t_1 \sim t_2$]**: At $t=t_1$, the primary-side current $i_p(t)$ linearly increase to zero, and the switch S_1 is conducted. As shown in mode 1, zero voltage turn-on of the switch S_1 is guaranteed because the anti-paralleled diode of S_1 is conducted. In this mode, the current $i_m(t)$ continues to increase and the output diode D_o continues to be bias-reversed. In this mode, all of the circuit equations are the same as those in operation mode 1.

Mode 3 **[$t_2 \sim t_3$]**: At $t=t_2$, the switches S_1 is turned off and $i_P(t)$ charges the output capacitor of the switch S_1 and discharges the output capacitor of the switch S_2. Because the output capacitors of the switches S_1 and S_2 are very small, the charging time and discharging time are very short. In this mode, the primary-side current $i_P(t)$ is recognized as being kept constant.

Mode 4 **[$t_3 \sim t_4$]**: At $t=t_3$, the voltage of the output capacitor for the switch S_1 is charged to the input voltage. Then, the voltage of switch S_2 is discharge to zero, and the anti-paralleled diodes of S_2 is forward-biased and turned-on to provide the following path for the primary-side current $i_p(t)$. Then, the voltage across the primary-side of the transformer is clamped to $-V_{cb}$, the magnetizing inductor current $i_m(t)$ decreases linearly from positive with a current slope of $(-V_{cb})/L_m$. In addition, at the secondary-side of the transformer, the output diode D_o is conducted due to the forward-bias of the diodes on the condition of the positive reflected secondary-side voltage V_{cb}/n. Then, the current through the output inductor is decreased with a current slope of $(-V_o)/L_o$, $i_{Lo}(t)$, which can be expressed as:

$$i_{Lo}(t) = i_{Lo}(t_3) - \frac{V_o}{L_o}(t-t_3) \quad (9)$$

At the secondary-side, the circuit equation can be obtained as:

$$L_{r2}\frac{di_s(t)}{dt} = \frac{-V_{cb}}{n} - v_{cr}(t) \quad (10)$$

$$i_s(t) = C_r\frac{dv_{cr}(t)}{dt} \quad (11)$$

Then, it is possible to obtain:

$$i_s(t) = i_s(t_3)\cos[\omega_r(t-t_3)] + \frac{-V_{cb}/n - v_{cr}(t_3)}{Z_r}\sin[\omega_r(t-t_3)] \quad (12)$$

$$v_{cr}(t) = -V_{cb}/n + Z_r i_s(t_3)\sin[\omega_r(t-t_3)] - [-V_{cb}/n - v_{cr}(t_3)]\cos[\omega_r(t-t_3)] \quad (13)$$

Where, $\omega_r=1/\sqrt{L_{r2}C_r}$ and $Z_r=\sqrt{L_{r2}/C_r}$. According to equation (12), the transformer secondary-side current $i_s(t)$ varies with a sinusoidal-shape. Therefore, there exist two cases. In the first case, the current $i_s(t)$ can be returned to zero and zero current turned-off for the diode D_o is achieved when the switch S1 is turned-off, and then the output inductor current $i_{Lo}(t)$ is equal to the current $i_s(t)$. In the second case, when the switch S_1 is turned-off, the current $i_s(t)$ cannot return to zero, and then the output inductor current $i_{Lo}(t)$ is larger than the current $i_s(t)$. In order to obtain ZCS for the diode, the first case is analyzed in the following.

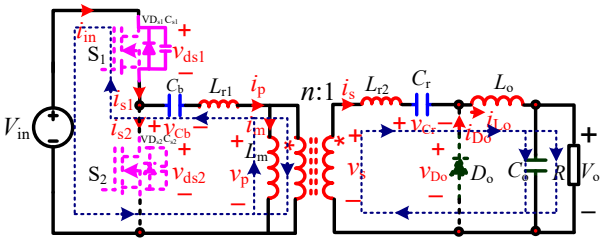
Mode 5 **[$t_4 \sim t_5$]**: At $t=t_4$, the primary-side current $i_p(t)$ decrease to zero from the positive to the negative, and then the switch S_2 is turned-on. The zero voltage turned-on for the switch S_2 is achieved due to the conduction of the anti-parallel diode of S2 in mode 4. After the switch S_2 is turned-on, the current im(t) continues to decrease, and the output diode D_o conducts. In addition, the current $i_{Lo}(t)$ through the output inductor continues to decreased with a current slope of $(-V_o)/L_o$, and the equation is the same as equation (9).

Mode 6 **[$t_5 \sim t_6$]**: At $t=t_4$, the resonant current $i_s(t)$ is equal to the output inductor current $i_{Lo}(t)$ and zero current turned-off for the diode D_o is achieved. The circuit equation is similar to that of mode 1. Then:

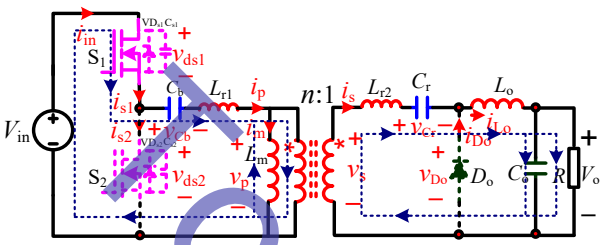
$$i_s(t) = i_{Lo}(t) = i_s(t_5) + \frac{(-V_{cb}/n - V_o) - v_{cr}(t_5)}{L_o}(t-t_5) \quad (14)$$

$$v_{cr}(t) = v_{cr}(t_5) + \frac{i_s(t_5)}{C_r}(t-t_5) \quad (15)$$

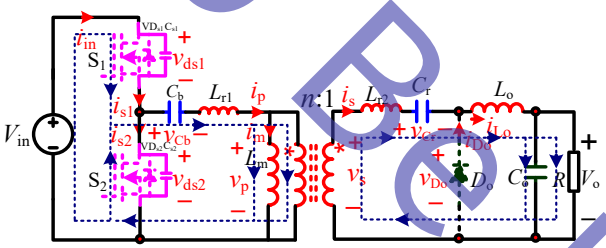
Mode 7 **[$t_6 \sim t_7$]**: At $t=t_6$, the switch S_2 is turned off and $i_P(t)$ charges the output capacitor of the switch S_2, and discharges the output capacitor of the switch S_1. When the output capacitors of the power switch S_2 is charged to the input voltage V_{in}, the anti-paralleled diode of the switch S_1 is conducted and the next switching cycle begins.



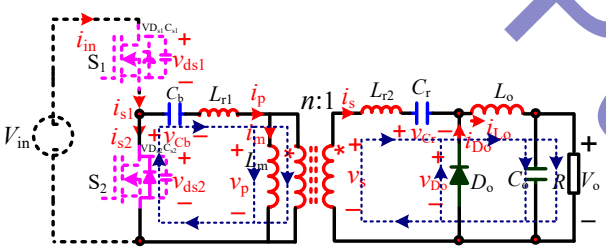
(a) Mode 1 [t_0~t_1].



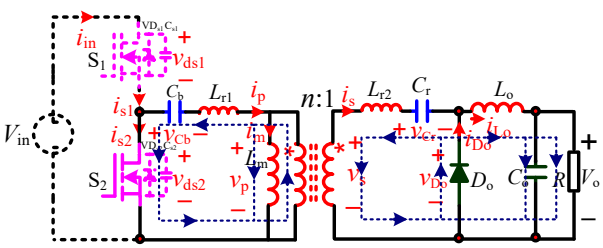
(b) Mode 2 [t_1~t_2].



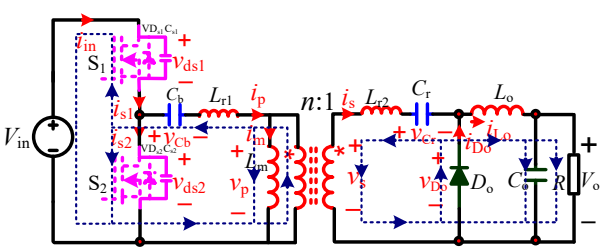
(c) Mode 3 [t_2~t_3].



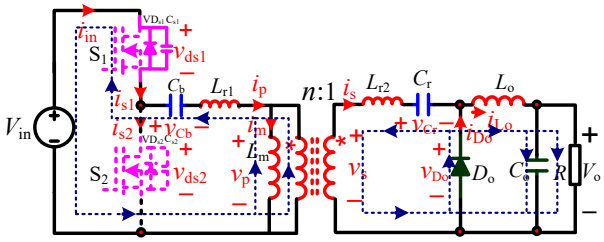
(d) Mode 4 [t_3~t_4].



(e) Mode 5 [t_4~t_5].



(f) Mode 6 [t_5~t_6].



(g) Mode 7 [t_6~t_7].

Fig.2 Operational modes of the proposed converter.

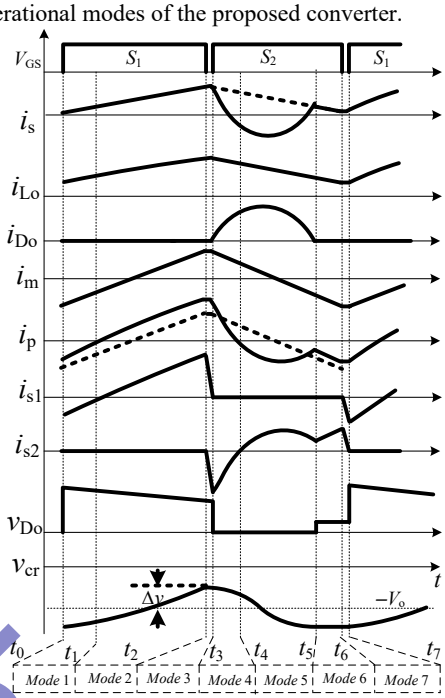


Fig.3 Key waveforms of the proposed converter.

III. Steady State Analysis

A. Voltage Transfer Gain

Assume the dead times in mode 3 and mode 7 are so short that they can be neglected. From the previous analysis, the voltage across the transformer primary side is $V_{in}-V_{cb}$, and in mode 4, mode 5 and mode 6, the voltage across the transformer primary side is $-V_{cb}$, where V_{cb} is the average voltage across the blocking capacitor C_b.

In the steady state, by applying the volt-second balance to the magnetizing inductor L_m, the average voltage across the clamp capacitor is given as:

$$(V_{in}-V_{cb})DT_s-V_{cb}(1-D)T_s=0 \tag{16}$$

And then:

$$V_{cb}=DV_{in} \tag{17}$$

Due to the volt-second balance of the inductors L_o, L_m and L_r, the average voltage across the resonant capacitor is equal to the output voltage, i.e. $V_{cr}=-V_o$. Then, the voltage across the output diode can be obtained as:

$$v_{Do}(t)=\begin{cases}\dfrac{V_{in}-V_{cb}}{n}-v_{cr}(t)-L_{r2}\dfrac{di_s(t)}{dt}, & t\in[t_0,t_3]\\ 0, & t\in[t_3,t_5]\\ \dfrac{-V_{cb}}{n}-v_{cr}(t)-L_{r2}\dfrac{di_s(t)}{dt}, & t\in[t_5,t_7]\end{cases} \quad (18)$$

Where:

$$L_{r2}\frac{di_s(t)}{dt}=L_{r2}\frac{[(V_{in}-V_{cb})/n-V_o]-v_{cr}(t_0)}{L_o}=K_1,\ t\in[t_0,t_3]$$

$$L_{r2}\frac{di_s(t)}{dt}=L_{r2}\frac{(-V_{cb}/n-V_o)-v_{cr}(t_5)}{L_o}=K_2,\ t\in[t_5,t_7]$$

Because the proposed converter operates in the steady state, in one switching period, the average voltage across the output diode D_o is equal to V_o with the volt-second balance of the inductor L_o. Thus, integral equation (18) and solve these equations, and the output voltage V_o can be obtained as:

$$V_o=\frac{DV_{in}}{n}-\frac{D}{1-D}K_1+\frac{-DV_{in}/n-K_2}{1-D}\frac{\Delta t_{57}}{T_s}-\frac{1}{(1-D)T_s}\int_{t_5}^{t_7}v_{cr}(t)dt \quad (19)$$

Where, $\Delta t_{57}=t_7-t_5$. In reality, in order to achieve ZCS for the diode D_o, the resonant frequency f_r must be slightly larger than the switching frequency f_s. Thus, the time interval Δt_{57} is short. Then, the voltage across the resonant capacitor can be considered as constant, and equation (19) can be simplified as:

$$V_o=\frac{DV_{in}}{n}-\frac{D}{1-D}K_1-\frac{K_2}{(1-D)}\frac{\Delta t_{57}}{T_s}+\frac{-DV_{in}/n+V_o+\Delta v}{1-D}\frac{\Delta t_{57}}{T_s} \quad (20)$$

In addition, from equation (6), the voltage ripple of the resonant capacitor can be expressed as:

$$\Delta v=\frac{I_o-\dfrac{V_o}{2L_o}(1-D)T_s}{2C_r}DT_s \quad (21)$$

Furthermore, the output inductor L_o is so large that the current ripple can be neglected. Then the half-sinusoidal wave through the diode D_o can be considered. Thus $\Delta t_{57}=(1-D)T_s-T_r/2$, where T_s and T_r are the switching period and the resonant period, respectively. Therefore, the voltage transfer gain of the proposed converter can be expressed as:

$$M=\frac{V_o}{V_{in}}=\frac{\dfrac{D}{n}}{1-\dfrac{T_s}{L_o}\dfrac{DT_s}{2C_rD_r}(Q-\dfrac{1-D}{2})(1-D-D_r)} \quad (22)$$

Where, the quality factor $Q=L_o/RT_s$ and $D_r=T_r/(2T_s)$. The parameter quality K is defined as:

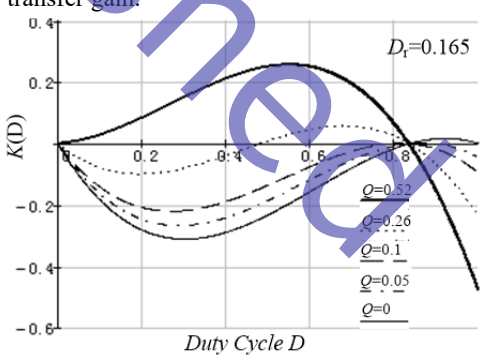
$$K=\frac{T_s}{L_o}\frac{DT_s}{2C_rD_r}(Q-\frac{1-D}{2})(1-D-D_r) \quad (23)$$

Thus, equation (22) can be simplified as:

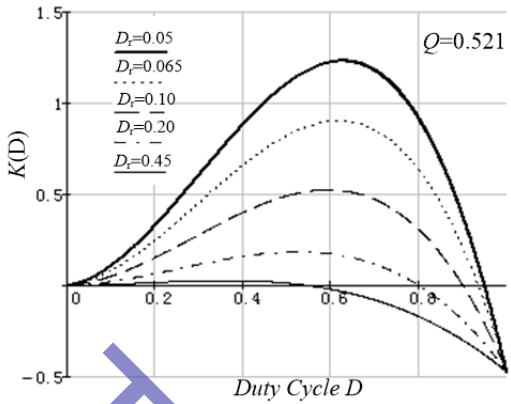
$$M=\frac{V_o}{V_{in}}=\frac{D/n}{1-K} \quad (24)$$

When the resonant duty cycle D_r is fixed, the curves are plotted as the parameter quality K versus the duty cycle D and the quality factor Q, as shown in Fig.4(a). From Fig.4(a), when the duty cycle D is smaller than 0.835, the amplitude of the parameter quality K is in the range of [–0.3, 0.3] with a variable duty cycle D and a quality factor Q. When D is larger than 0.835, the parameter quality K varies sharply. When the quality factor Q is fixed, the curves are plotted as the parameter quality K versus the duty cycle D and the quality factor D_r, as shown in Fig.4(b). From Fig.4(b), the parameter quality K increases when D_r decreases and D increases. However, the parameter quality K behaves as a parabolic-wave property. When D gets larger, the parameter quality K is decreased.

From equation (24), the curves of the voltage transfer gain of the proposed converter are shown in Fig.5. Fig.5(a) plot the curves of the voltage transfer ratio M versus D and Q with a constant D_r, when the resonant duty cycle D_r is fixed. As can be seen from Fig.5(a), the proposed converter nearly has the same linear voltage transfer gain characteristics as the buck-type converter when D_r is constant. When the load get lighter, the linearity of the characteristic is better. When the quality factor is fixed, the curves of the voltage transfer ratio M versus the duty cycle D and D_r is shown in Fig.5(b). As can be seen from Fig.5(a), in order to obtain the linearity voltage gain of the proposed converter, the resonant duty cycle D_r should be large but should not exceed the duty cycle with ZCS for the output diode, and the parameter of Q should be kept smaller at the maximum power to keep the linearity of voltage transfer gain.

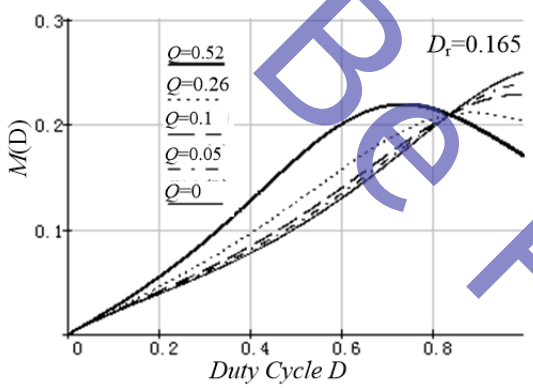


(a)

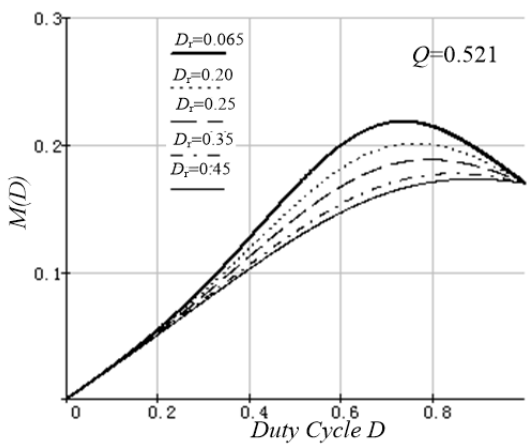


(b)

Fig.4 Curves of the parameter quality K: (a) the parameter quality K versus D and Q with a constant D_r; (b) the parameter quality K versus D and D_r with a constant Q.



(a)



(b)

Fig.5 Curves of the voltage transfer ratio M: (a) the voltage transfer ratio M versus D and Q with a constant D_r; (b) the voltage transfer ratio M versus D and D_r with a constant Q.

IV. PERFORMANCE ANALYSIS

A. ZCS Condition for the output diode

From the above operational mode analysis, the ZCS condition for the output diode D_o is achieved when the resonant current $i_s(t)$ is equal to the output inductor current $i_{Lo}(t)$ before the switch S_2 is turned-off. The sinusoidal-wave for the output diode is considered due to the current ripple of the output inductor being neglected with a large inductance value. Thus, the ZCS condition for the output diode can be obtained as:

$$\frac{1}{2f_r} < (1-D)T_s \tag{25}$$

Based on the expression of equation (21), the resonant capacitor C_r can be obtained as:

$$C_r = \frac{I_o - \frac{V_o}{2L_o}(1-D)T_s}{2\Delta v} DT_s \tag{26}$$

Fig.6 shows the curves resonant capacitor value versus the duty cycle D with a quality factor of Q=0.5, f_s=50kHz and L_o=100μH. As can be seen from Fig.6, when the voltage ripple is below 20 percent of the output voltage, the capacitor value can be selected below 5μF in the entire duty cycle range. Thus, ceramic or film capacitors with a small equivalent series resistance can be selected.

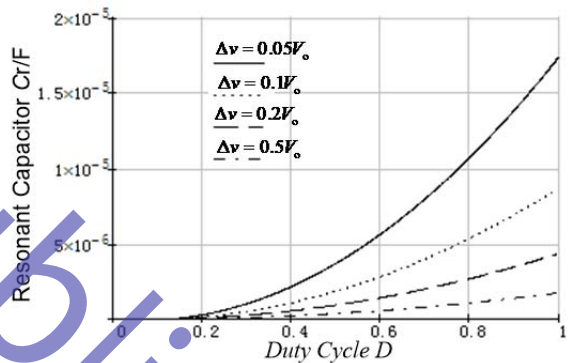


Fig.6 Curves of the resonant capacitor selection.

When the resonant capacitor is obtained according to equation (26), the resonant inductor can be achieved from equation (25) as:

$$L_{r2} < \frac{(1-D)^2 T_s^2}{\pi^2 C_r} \tag{27}$$

B. ZVS Condition for the primary-side power switches

Based on operation principle of the proposed converter in the section II, in order to achieve zero-voltage turned-on for the power switches, the output capacitor voltage of the switches S_1 and S_2 should be charged or discharged to zero in the dead time. In addition, the key waveforms of the proposed converter, as shown in Fig.3, indicate that the current through the primary-side of the transformer is positive at the time t_2, and ZVS for the switch S_2 can be achieved. Furthermore, the current through the primary-side of the transformer is negative at the time t_6, and ZVS for the switch S_1 can be achieved. Thus, ZVS condition for the switches S_1 and S_2 can be expressed as:

$$-I_{\mathrm{m}}(t_6)+I_{\mathrm{Lo,min}}<0 \tag{28}$$

$$I_{\mathrm{m}}(t_2)+I_{\mathrm{Lo,max}}>0 \tag{29}$$

Where, $I_{\mathrm{m}}(t_2)$ and $-I_{\mathrm{m}}(t_6)$ are the maximum and minimum of the magnetizing inductor current i_{m}. Because there exists a blocking capacitor in the primary-side of the transformer, no bias current get through the magnetizing inductor. Thus, $I_{\mathrm{m}}(t_2)= I_{\mathrm{m}}(t_6)=V_{\mathrm{in}}*D(1-D)T_{\mathrm{s}}/(2L_{\mathrm{m}})$. In the proposed converter, the average of the output inductor current i_{Lo} is equal to the output current I_{o} ($I_{\mathrm{Lo}}=I_{\mathrm{o}}$). Thus, $I_{\mathrm{Lo,max}}$ and $I_{\mathrm{Lo,min}}$ can be expressed as $I_{\mathrm{Lo,max}}=(1+\Delta I/I_{\mathrm{o}}*100\%)I_{\mathrm{o}}$ and $I_{\mathrm{Lo,max}}=(1-\Delta I/I_{\mathrm{o}}*100\%)I_{\mathrm{o}}$. Therefore, the ZVS condition for the switches S_1 and S_2 can be obtained as:

$$-\frac{V_{\mathrm{in}}D(1-D)T_{\mathrm{s}}}{2L_{\mathrm{m}}}+(1-\frac{\Delta I}{I_{\mathrm{o}}}\cdot 100\%)\cdot I_{\mathrm{o}}<0 \tag{30}$$

$$\frac{V_{\mathrm{in}}D(1-D)T_{\mathrm{s}}}{2L_{\mathrm{m}}}+(1+\frac{\Delta I}{I_{\mathrm{o}}}\cdot 100\%)\cdot I_{\mathrm{o}}>0 \tag{31}$$

Based on equations (30) and (31), the ZVS for the switch S_2 can be achieved during the entire load range. In addition, in order to achieve ZVS turned-on for the switch S_1, the magnetizing inductor can be satisfied by the following inequality equation:

$$L_{\mathrm{m}}<\frac{V_{\mathrm{in}}D(1-D)T_{\mathrm{s}}}{2(1-\Delta I/I_{\mathrm{o}}\cdot 100\%)\cdot I_{\mathrm{o}}} \tag{32}$$

Thus, equation (32) is satisfied when the rated power is given and the output current I_{o} is decided. At this moment, the maximum magnetizing inductor can be selected to achieve ZVS for the primary-side power switches S_1 and S_2.

C. Voltage stress for the power switches and diode

Based on the above analysis, it can be easily seen that the voltage stress of the power switches S_1 and S_2 is clamped to the input voltage. It can be seen from equation (18), that the voltage stress for the output diode D_{o} can be obtained as:

$$\begin{aligned} V_{\mathrm{do,max}} &= \frac{V_{\mathrm{in}}-V_{\mathrm{cb}}}{n}+V_{\mathrm{o}}+\Delta v \\ &= \frac{V_{\mathrm{in}}}{n}[(1-D)+\frac{D}{1-K}]+\Delta v \end{aligned} \tag{33}$$

When the input voltage is selected as the base voltage, the voltage stress for the output diode can be expressed as:

$$\frac{V_{\mathrm{do,max}}}{V_{\mathrm{in}}/n}=(1-D)+(1+\frac{\Delta v}{V_{\mathrm{o}}}\cdot 100\%)\cdot nM \tag{34}$$

where, M is voltage transfer gain of the proposed converter and $\Delta v/V_{\mathrm{o}}$ is the ripple coefficient of the output voltage.

Fig.7 describes the curves of the voltage stress of the output diode D_{o} versus the duty cycle D with Δv=20%V_{o}. It can be seen from Fig.7 that the voltage stress for the output diode D_{o} is always below $1.15V_{\mathrm{in}}/n$ in the entire duty cycle range. In addition, the voltage stress of the output diode D_{o} varies slowly vs. the duty cycle. The reason can be explicated that in order to get a constant output voltage when the input voltage decreases, the voltage transfer gain is at its maximum, but the duty cycle D is large. Inversely, when the input voltage increases, voltage transfer gain is at its minimum, but the duty cycle D is small. Therefore, the duty cycle D seldom has an influence on the voltage stress of the output diode. Comparing the traditional asymmetric half bridge converter with the forward-type rectifier, the voltage stress for the output diodes are $V_{\mathrm{in}}/(\mathrm{n}D)$ *and* $V_{\mathrm{in}}/(n(1-D))$, respectively. It can be obtained that in the traditional AHB converter topology, the voltage stresses for the output diode varies with the duty cycle. Therefore, the proposed converter has preferred performance with a nearly constant voltage stress for the output diode.

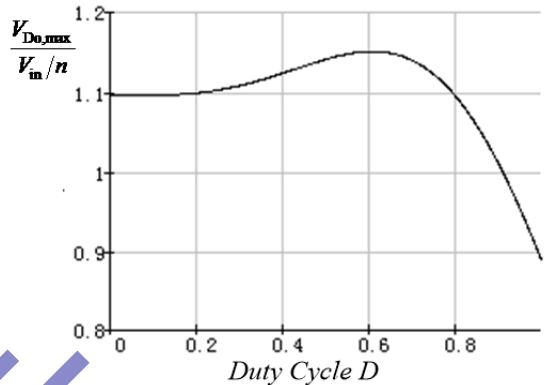


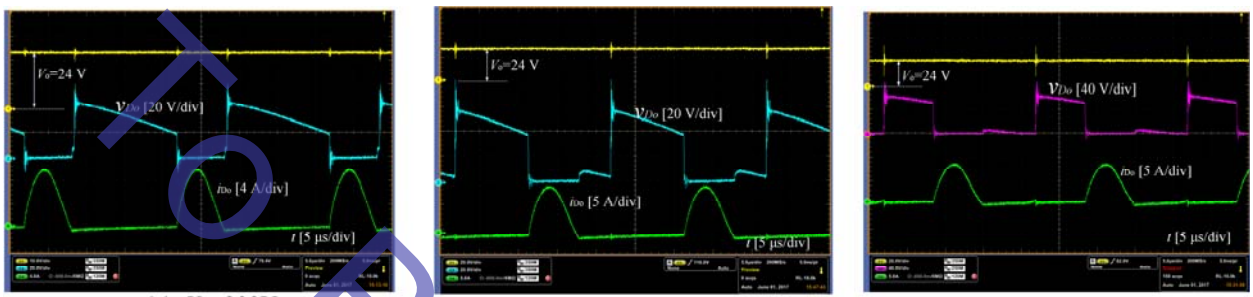
Fig. 7 Curves of the diode voltage stress selection.

V. Experimental Results

Experimental studies of the proposed converter have been performed to verify the above analysis results with the converter parameters as: 1) input voltage V_{in}=200V～380V; 2) output voltage V_{o}=24V; 3) maximum output power P_{o}=50W; 4) switching frequency f_{s}=50kHz, output inductor L_{o}=100μH, and output capacitor C_{o}=200μF.

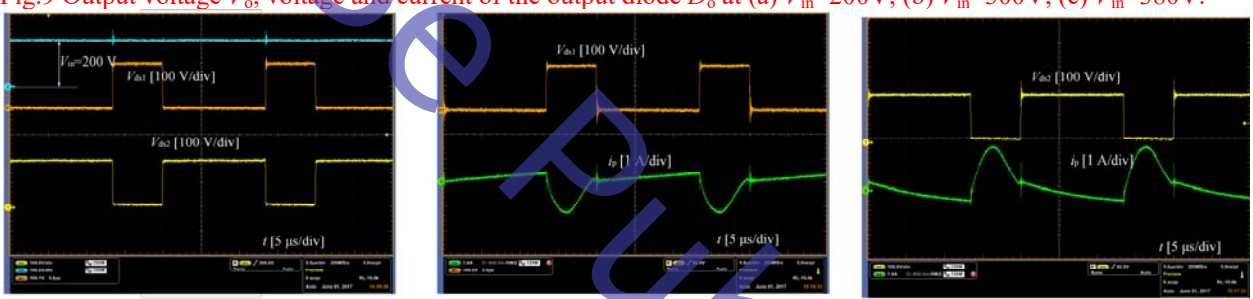
Based on the above analysis, in order to achieve ZCS for the diode D_{o}, the resonant frequency should be larger than the switching frequency. In addition, when f_{r} become very large, the conduction losses of the power switch and diode for the proposed converter are dominant and decrease the performance of the converter. Thus, for a trade-off between the conduction losses and ZCS condition of diode, a resonant duty cycle D_{r} equal to 0.3 is selected to guarantee the ZCS of the output diode on the condition of the rated output power and the minimum input voltage. According to Fig.(6), the capacitance value of the resonant capacitor can be obtained on the condition of Δv=20%V_{o}. Thus, C_{r}=2.2μF was selected. When C_{r} is fixed, according to equation (27), the resonant inductor can be selected. A TDK ETD34 core is used for the design of the transformer. The primary and secondary turns

of the transformer are n_p= 26T and n_s=5T. The magnetizing inductance L_m=410μH is designed to achieve ZVS turned-on for the switches S_1 and S_2 according to equation (32). The secondary resonant inductor is L_{r2}=1.65μH. Then the resonant frequency $f_r = 1/2\pi\sqrt{L_r C_r}$ =83kHz. In addition, the quality factor is Q= 0.417 at a full load. The parameters of the passive components and semiconductors are shown in Fig.8 with the circuit parameters given in Table 1.



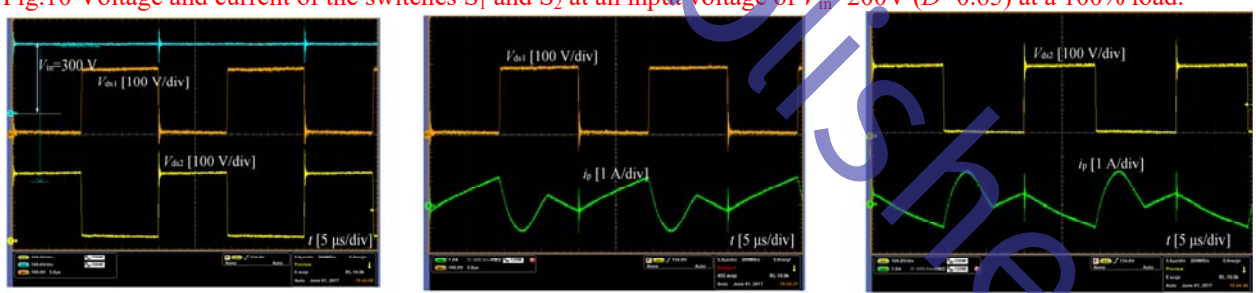
(a) V_{in}=200V (b) V_{in}=300V (c) V_{in}=380V

Fig.9 Output voltage V_o, voltage and current of the output diode D_o at (a) V_{in}=200V; (b) V_{in}=300V; (c) V_{in}=380V.



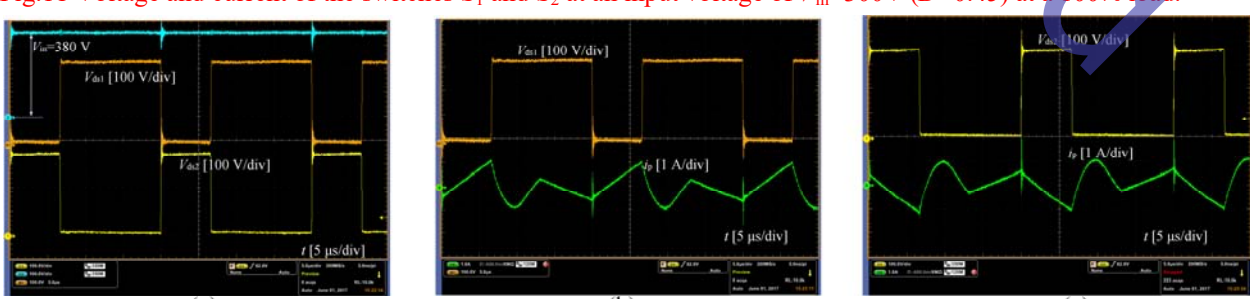
(a) (b) (c)

Fig.10 Voltage and current of the switches S_1 and S_2 at an input voltage of V_{in}=200V (D=0.65) at a 100% load.



(a) (b) (c)

Fig.11 Voltage and current of the switches S_1 and S_2 at an input voltage of V_{in}=300V (D=0.45) at a 100% load.



(a) (b) (c)

Fig.12 Voltage and current of the switches S_1 and S_2 at an input voltage of V_{in}=380V (D=0.32) at a 100% load.

Fig. 8 Photograph of an experiment prototype for the proposed converter.

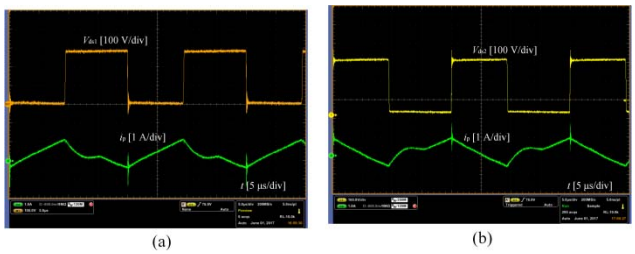
Table 1 - Parameters of the proposed converter

Main switches(S_1~S_2)	SPW11N60C3
diodes(D_o)	STTH2002C
Main Transformer	Core: ETD34 PC40 Trun Ratio: 26 : 5 *Manetizing inductance* L_m: 410μH Secondary resonant inductor L_{r2}: 1.65μH
Output inductor	
Blocking Capacitor (C_b)	1μF/600V
Output Capacitor (C_o)	200μF/100V
Resonant Capacitor (C_r)	2.2μF

A. Experimental Results

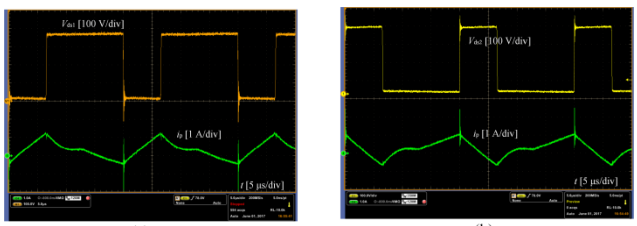
Fig. 8 shows a photograph of an experiment prototype for the proposed converter. The key waveforms of the proposed converter at the input voltage, *i.e.*, 200V, 300V, 380V, at a full load are given in Fig.9-Fig.12. Fig.9 shows experimental waveforms of the output voltage, and the voltage and current waveforms of the output diode. It can be seen from Fig.9 that before the diode is turned-off, the current through the output diode is decreased to zero. Therefore, ZCS for the diode is achieved under a wide input voltage through appropriate design of the resonant tank. Moreover, it can be seen that the voltage stress of the output diode varies in a narrow range under different input voltages.

Fig.10-Fig.12 show voltage and current waveforms for the switches S_1 and S_2 at different input voltages. It can be seen from Fig.10-Fig.12 that the anti-parallel diode for the switches S_1 and S_2 are conducted before the switches are turned-on. Thus, ZVS for the switches S_1 and S_2 can be achieved through appropriate design of the magnetizing inductor. Fig.13～Fig.15 show waveforms of the switches S_1 and S_2 at a 20% load under different input voltages. In addition, at light load, ZVS for the switches S_1 and S_2 can be obtained to eliminate the switching losses and to improve the efficiency of the proposed converter.



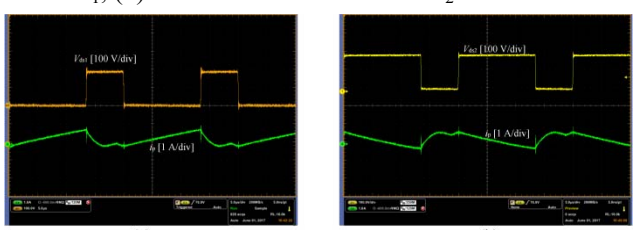
(a) (b)

Fig.13 V_{in}=200V and a 20% load: (a) waveforms for the switch S_1; (b) waveforms for the switch S_2.



(a) (b)

Fig.14 V_{in}=300V and a 20% load: (a) waveforms for the switch S_1; (b) waveforms for the switch S_2.



(a) (b)

Fig.15 V_{in}=380V and a 20% load: (a) waveforms for the switch S_1; (b) waveforms for the switch S_2.

B. Efficiency

Fig.16 shows the efficiency at an input voltage of 200 V. It can be seen from Fig. 10 that the proposed converter has a peak efficiency of 96.5%. At a light-load, the efficiency decreases because the switching-related losses of this converter are dominant. In addition, it can be seen from Fig.16 that at a full load, the efficiency of the proposed converter is slightly smaller than that of the traditional AHB converter. This is due to the fact that in order to obtain ZCS for the output diode and ZVS for the switch, the magnetizing inductor in the proposed converter is smaller than that in the traditional AHB converter. Therefore, additional circulating losses are dominant, but the reverse recovery loss for the output diode is eliminated in the proposed converter. Thus, the conduction loss and reverse recovery loss should be a trade-off. However, at a light load, the efficiency of the proposed converter is much higher than that in the traditional AHB converter. ZCS for the output diode and ZVS for the switch in the proposed converter are maintained in the entire load range. However, ZVS for the switch is lost in the traditional AHB converter.

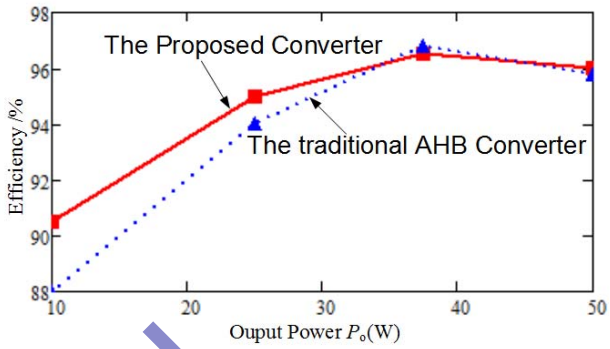


Fig. 16 Efficiency curves.

VI. CONCLUSIONS

This paper presented a secondary resonance half-bridge DC-DC converter with an inductive output filter. The operational principle, performance analysis and design equations of the proposed converter are given. Analysis results show that the output diode voltage stress is independent of the duty cycle, and that it achieves preferred performance with a nearly constant voltage stress for the output diode. In addition, the voltage gain is almost linear, which is similar to that of the isolation Buck-type converter. Experimental results of a prototype converter verify the theoretical analysis results. They show that ZVS switching for the switches and ZCS switching for the output diode are achieved in the entire load range. Based on these merits, the proposed converter is available for application, especially in the high-voltage applications such as high-voltage battery chargers (200–400 V), LED lighting, etc.

ACKNOWLEDGMENT

This work was supported by the National Natural Science Foundation of China under grant no.51607027, the Fundamental Research Funds for the Central Universities under project number ZYGX2016KYQD123, and the Scientific and Technical Supporting Programs of Sichuan Province under Grant (2016GZ0395, 2017GZ0391 and 2017GZ 0392).

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