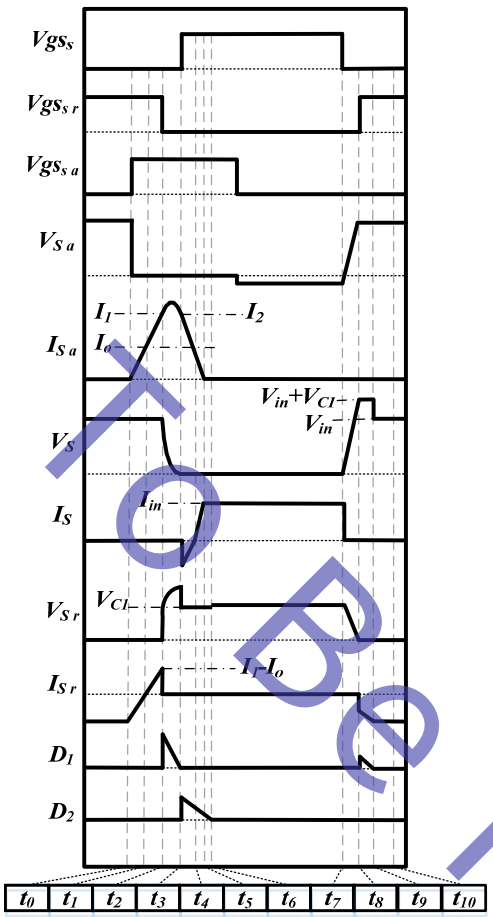

Fig. 3. Typical waveforms of the proposed converter

In this interval, D_2 starts to conduct. Thus, the capacitor of the clamp circuit discharges its extra energy. Important equations of this interval are expressed as follows:

$$I_{La} = I_2 - \frac{V_o - V_{C1}}{L_a}(t - t_3), \tag{9}$$

$$t_4 - t_3 = L_a \frac{(I_2 - I_{La})}{V_o - V_{C1}}. \tag{10}$$

At the end of this interval, L_a current decreases linearly to I_O, and the body diode of S is turned off.

Interval 5 [t_4–t_5], *Fig. 2(e):* The difference between the output and the capacitor of clamp circuit is placed across L_a given that main switch S is turned on. C_1 discharges its energy to the output through D_2 and L_2. The equations of L_a current and duration of this interval are expressed as follows:

$$I_{La} = I_o - \frac{(V_o - V_{C1})}{L_a}.(t - t_4), \tag{11}$$

$$t_5 - t_4 = \frac{I_o - I_{La}}{V_o - V_{C1}}. \tag{12}$$

At the end of this interval, the L_a current decreases linearly to zero, and I_S reaches I_{in} because the output and C_1 voltages are assumed constant in a switching cycle.

Interval 6 [t_5–t_6], *Fig. 2(f):* In this interval, main switch S remains on, and C_1 is discharged. At the end of this interval, V_{C1} reaches its initial value, and D_2 is turned off. The equation of V_{C1} at the end of this mode is expressed as follows.

$$V_{C1} \approx \frac{nV_{in} + V_O}{n+1} \tag{13}$$

Interval 7 [t_6–t_7], *Fig. 2(g):* L_1 and L_2 absorb the power from the input because the main switch is on, and the input energy is transmitted to the output. L_a current is zero. Thus, the auxiliary switch can be turned off under ZCS. Considering L_t as the total inductance of series coupled inductances L_1 and L_2, the current of L_1 and the duration of this mode are expressed as:

$$I_{L1} = \frac{(V_{in} - V_o)}{L_t}.(t - t_6), \tag{14}$$

$$t_7 - t_6 = \frac{I_{L1}.L_t}{V_{in} - V_o}. \tag{15}$$

Interval 8 [t_7–t_8], *Fig. 2(h):* In this interval, the main switch is turned off under the ZV condition because of the existence of snubber capacitance. Accordingly, C_s is charged, and its voltage reaches $V_{in}+V_{C1}$.

Interval 9 [t_8–t_9], *Fig. 2(i):* At the beginning of this interval, S_r body diode and D_1 start to conduct. Hence, the synchronous switch can be turned on under the ZV condition. The energy of L_1 is stored in C_1, and its current reduces linearly. The stress voltage of the main switch is clamped by the clamp capacitor. The current of L_2 and S_r body diode increases linearly. At the end of this interval, the current of L_1 becomes zero, and the current of S_r body diode and L_2 reaches I_O.

Interval 10 [t_9–t_{10}], *Fig. 2(j):* In this interval, the output current flows through S_r and L_2. This mode continues until the gate pulse of S_a is applied, and the next cycle of switching is started.

III. DESIGN CONSIDERATION

The proposed converter is designed for 150 V input voltage, 24 V output voltage, and 100 W output power at 100 kHz switching frequency. The conversion gain is obtained using the L_1 volt-second balance, which is expressed by:

$$\frac{V_o}{V_{in}} = \frac{D}{1 + \frac{1}{n}(1 - D)}, \tag{16}$$

where n is n_2/n_1. Fig. 4 depicts the curves of voltage gain versus the duty cycle of the proposed converter for various turn ratio n.

The total inductance of series coupled inductor L_t, which is equal to $(1+1/n)^2$. L_2 can be calculated similarly to a regular buck converter. Thus, L_2 can be written as

$$L_2 = \frac{(V_i - V_O)D}{(1 + \frac{1}{n})^2 . f_{sw} . \Delta i_L}. \tag{17}$$

The relationship between L_2 and L_1 is determined by the

turn-ratio of the magnetic element.

$$\frac{L_2}{L_1} = (\frac{n_2}{n_1})^2 = n^2 \qquad (18)$$

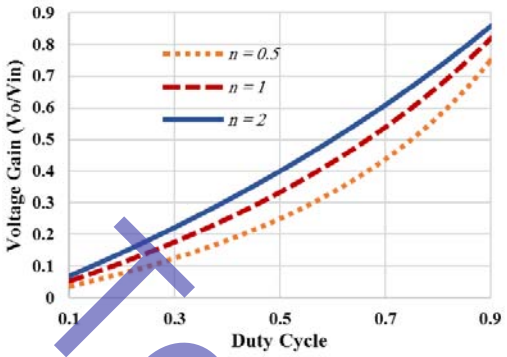

Fig. 4. Gain voltage of the proposed converter for various n

For a given gain, the values of L_1 and L_2 are determined according to (17) and (18), as summarized in Table I, for $n = 1$. Low output voltage leads to a low value of n. In this case, the L_1 value can be increased to avoid a minimal value of L_2, which indicates that inductor current ripple Δi_L is not increased according to (17).

The design of snubber capacitor C_s is similar to other regular turn-off snubber capacitors [24].

$$C_{S_{\min}} = \frac{I_{SW}.t_f}{2.V_{SW}} \qquad (19)$$

where I_{SW} is the switch current before turn off, V_{SW} is the voltage after turn off, and t_f is the switch current fall time. C_S is selected with a larger value than C_{Smin} to ensure the soft-switching condition.

The value of L_a is similar to a regular turn-on snubber inductor [24], which should satisfy the following relation to guarantee the soft-switching condition:

$$\frac{1}{2}.L_a.(I_1 - I_o)^2 \geq \frac{1}{2}.C_S.(V_{in} + V_{C1})^2 . \qquad (20)$$

The control circuit is designed similar to its hard-switching counterpart through a PWM controller. The scheme depicted in Fig. 5 is used to achieve the required timings for each switch pulse and adjust the PWM controller pulse for three switches. The soft-switching condition is provided from minimum to full load similar to other soft-transition converters because delay times are fixed for the worst case.

IV. Experimental Waveforms and Efficiency

A 100 W, 150–24 V prototype of the proposed converter at 100 kHz switching frequency is constructed to verify the theoretical analysis and key waveforms. The passive component values are listed in Table I. IRF740 is selected for the main switch, S and IRF640 are utilized for S_a and S_r, S_a contains a series diode to act as a unidirectional auxiliary switch. D16S60C is used for diodes. The photo of the prototype is depicted in Fig. 6 The voltage and current waveforms are measured using Tektronix TDS2014c oscilloscope and PINTEK PA-677 current probe. Fig. 7 displays the voltage and current waveforms of the main switch and its turn-on and turn-off instants, which confirm the ZVT operation of the main switch.

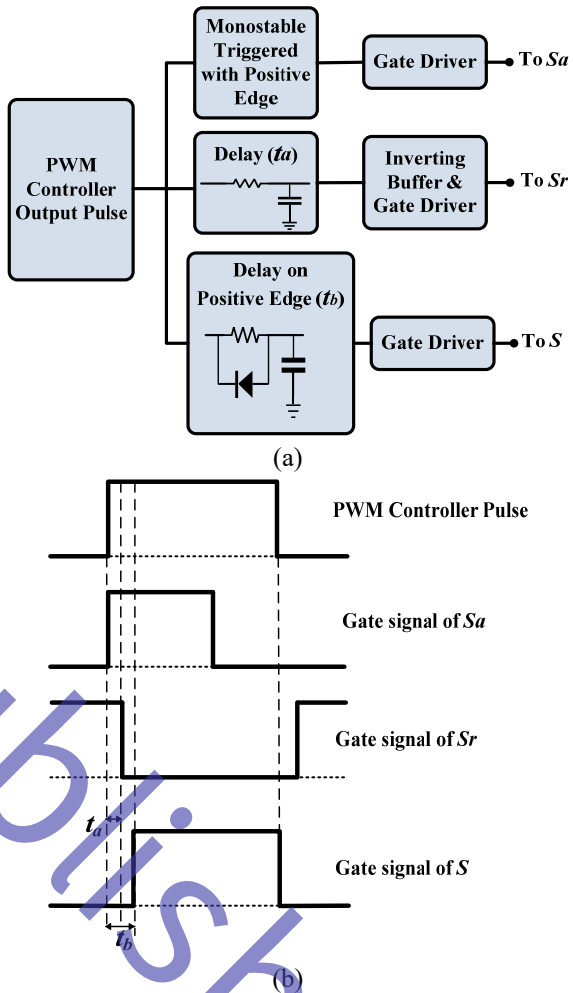

Fig. 5. (a) Driver circuit, (b) Timing diagram

Fig. 6. Photo of the proposed converter prototype

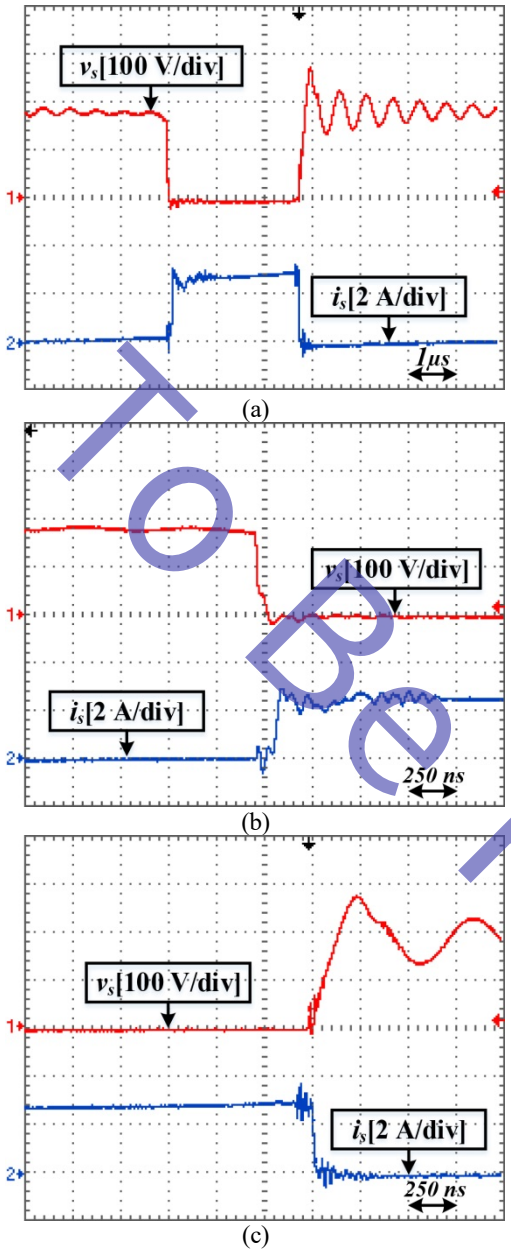

Fig. 7. (a) Voltage (top) and current (bottom) waveforms of the main switch, (b) turn-on instant, (c) turn-off instant

TABLE I

COMPONENT VALUES OF THE PROTOTYPE

Component	Value
L_1, L_2	300 μH
C_1	10 μF
C_s	2.2 nF
C	100 μF
L_a	3 μH

In Fig. 7 (b), the body diode of the main switch is conducted before the switch turn on. The snubber capacitor provides the ZV condition for turning off, as demonstrated in Fig. 7 (c). In Fig. 7, the voltage spike caused by the leakage inductance of the coupled inductor is clamped by the clamp circuit. Fig. 8 (a) displays the ZCS operation of the auxiliary switch. The auxiliary switch turns on and off under ZCS. The voltage and current of synchronous switch S_r is illustrated in Fig. 8 (b). S_r turn on is under ZV, as discussed in the theoretical analysis. Furthermore, the current waveforms of D_1 and D_2 are shown in Figs. 9 (a) and (b), correspondingly.

The semiconductor device losses of the prototype are tabulated in Table II. Fig. 10 illustrates the efficiency curve of the proposed converter and hard-switching buck converter with a tapped inductor. A unidirectional switch can be used rather than series diode (D_a) and S_a to reduce the conduction loss caused by this series diode.

TABLE II

SEMICONDUCTOR LOSSES IN THE PROPOSED CONVERTER

Type of loss	Element	Loss (W)
Conduction losses of switches (W) $R_{ds}.f_{sw}.\int_T I_s^2 dt$	S	0.9
	S_a	2.1
	S_r	3.12
Capacitive losses of switches (W) $\frac{1}{2}.C_o V_{ds}^{\ 2} f_{sw}$	S	0.08
	S_a	0.05
	S_r	0.075
Conduction losses of diodes (W) $I_{ave}.V_F$	D_1	0.005
	D_2	0.01
	D_a	1.2

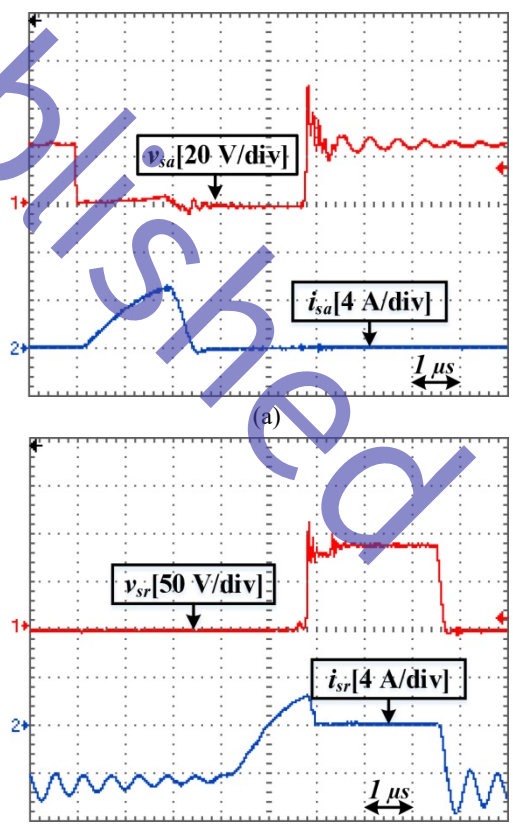

Fig. 8. Experimental voltage and current waveforms: a) S_a, b) S_r

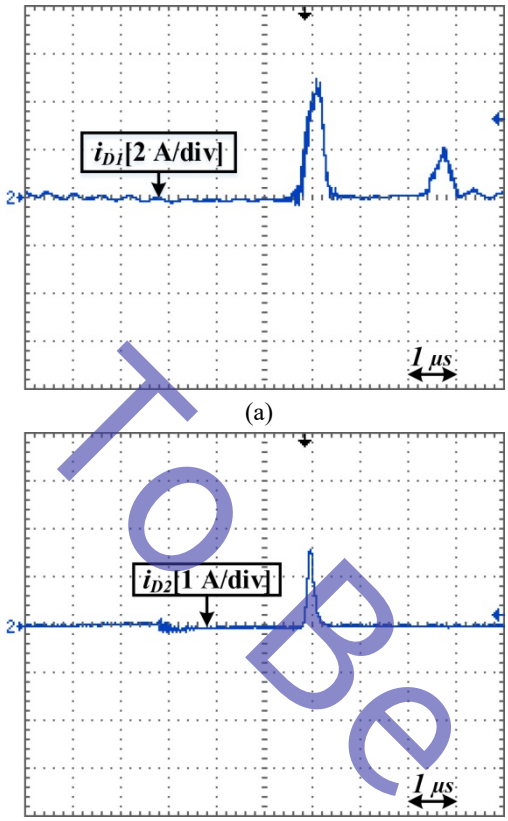

Fig. 9. Experimental result waveforms: a) D_1 current, b) D_2 current

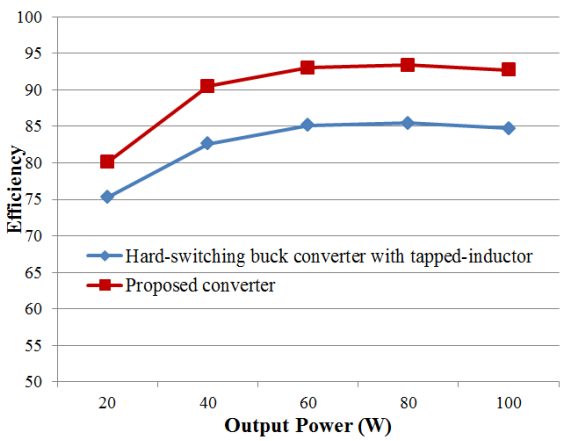

Fig. 10. Efficiency curves of the proposed converter and hard-switching buck converter with tapped inductor

V. Conducted EMI Measurement

In this section, the experimental measurement of conducted EMI for the proposed converter and its hard-switching counterpart with a tapped inductor is evaluated. Conducted electromagnetic emissions are measured according to the CISPR 22 standard. CISPR 22 line impedance stabilization network (LISN) is inserted between the converters and input lines. The measured conducted EMI for the hard-switching buck converter with a tapped inductor and the proposed converter are displayed in Figs. 11(a) and 10(b), respectively, using GW-Instek GSP830 spectrum analyzer. In Fig. 11, the main conducted EMI peak for the hard-switching buck and proposed converters are approximately 91 and 84 dBμV, respectively, indicating that the main peak of the proposed converter is reduced in terms of its hard-switching counterpart by providing soft-switching and clamp techniques. For further EMI comparison, Fig. 12 compares EMI peaks in various frequency bands. According to CISPR 22 Class *A* limit (79 dBμV for 0.15–0.5 MHz and 73 dBμV for 0.5–30 MHz frequency band), the EMI levels of the proposed converter are under the standard limit (73 dBμV) at approximately 13–30 MHz frequency band, whereas its hard-switching converter has an EMI level higher than the standard limit in most frequency bands. The proposed converter contains several frequencies below 13 MHz with higher values than CISPR 22. An EMI filter with low characteristics and attenuation can be used for 0.15–13 MHz to satisfy CISPR 22 at this frequency band because the emission levels are significantly reduced in the proposed converter with respect to its hard-switching counterpart.

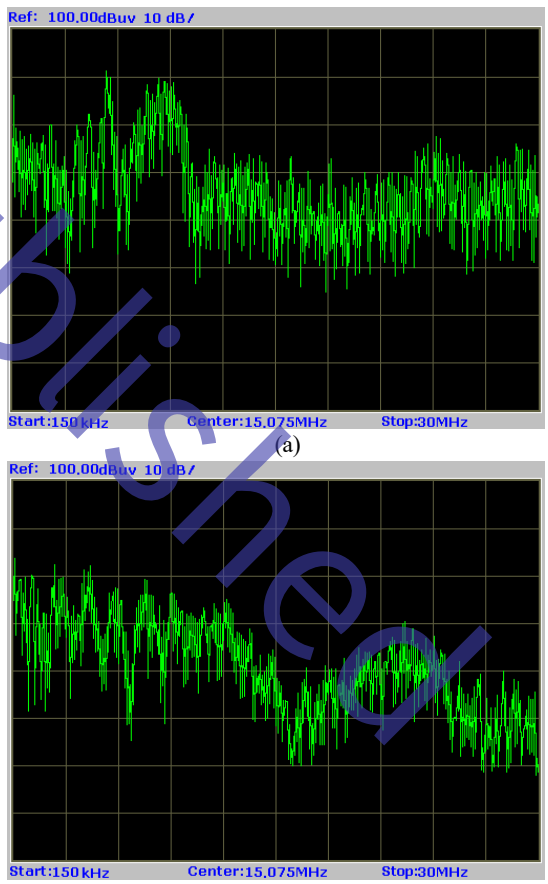

Fig. 11. Conducted EMI measurement of a) hard-switching buck converter with tapped inductor b) proposed converter (Ver. axis: 20–100 dBμV, Hor. axis: 0.15–30 MHz)

TABLE III
COMPARISON OF HIGH STEP-DOWN ZERO-VOLTAGE CONVERTERS (V_{IN} = 150 V, V_O = 24 V, P_O = 100 W)

Converter	Efficiency (%)	EMI Peak (dBμV)	Number and Value of Elements				Switching condition					
			Switch	Diode	Magnetic Core	Capacitor	Main switch		Another switch		Synchronous switch	
							ON	OFF	ON	OFF	ON	OFF
[18]	89	90.5	2	2	No.: 2 Coupled Inductor Small Inductor (<10 μH)	No.: 3 10 μF, 50 μF, 2400 μF	ZV	Hard	ZV	Hard	Without Sync. Switch	
[20]	88.5	96.7	3	0	No.: 2 Coupled Inductor Large Output Inductor	No.: 3 20 μF, 40 μF, 660 μF	ZV	Hard	ZV	Hard	Nearly ZV	Hard
[25]	91.3	93.1	2	0	No.: 1 Coupled Inductor	No.: 1 100 μF	ZV	Hard	Without Aux. Switch		ZV	Hard
This Work	92.5	87	3	2	No.: 2 Coupled Inductor Small Inductor (<10 μH)	No.: 3 2.2 nF, 10 μF, 100 μF	ZV	ZV	ZC	ZC	ZV	Hard

VI. COMPARISON WITH OTHER HIGH STEP-DOWN ZV CONVERTERS

A comparison between the proposed and another ZVS high step-down converters is presented in Table III. All converters are designed with components and specifications similar to the proposed converter. In addition to efficiency at nominal load, the conducted EMI of converters and the proposed converter is simulated using LISN and the converter circuit model in OrCAD. Instead of the measured EMI peak value, The simulated EMI peak value of the proposed converter is shown, rather than its measured EMI peak, because the EMI of [18], [20], and [25] are simulated value. The converter in [25] can only operate in the CRM and has a limitation for soft-switching operation area versus load range, although it had fewer components than other converters. Similar to other soft-transition converters, the soft-switching condition is independent of load changes in the proposed converter compared with regular resonant converters. In [20], high-frequency spikes occur across the synchronous switch caused by leakage inductance, yielding much EMI, which is confirmed by a simulated EMI peak. In addition to enhanced efficiency, the EMI simulation shows that the proposed converter has lower EMI peak due to better soft-switching conditions at switching instants over the abovementioned converters.

VII. CONCLUSIONS

In this study, a soft-switching high step-down converter with an auxiliary cell, a lossless clamp circuit, and a synchronous rectifier where its duty cycle is extended by a coupled inductor is proposed. The theoretical and experimental results indicate that the main switch turns on and off under the ZV condition. The turn-on of the synchronous switch is ZV, and the auxiliary switch turn-on and turn-off are under ZC. A lossless clamp limits the voltage spike of the main switch generated by leakage inductance in buck converters with a coupled inductor and recovers its energy. The efficiency of the proposed converter is improved compared with the hard-switching buck converter with a tapped inductor and other similar ZV converters. Furthermore the proposed converter exhibited a lower EMI peak than the hard-switching and three similar ZV converters.

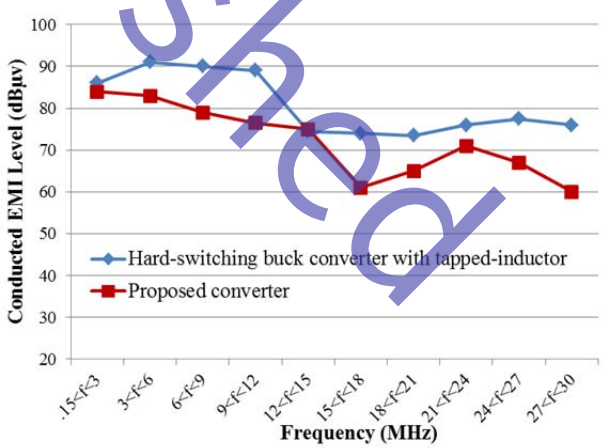

Fig. 12. Comparison of conducted EMI peaks in various frequency bands – experimental results

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