Fundamental Output Voltage Enhancement of Half-Bridge Voltage Source Inverter with Low DC-link Capacitance

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Abstract

Conventionally, in order to reduce the ac components of the dc-link capacitors of the two-level Half-Bridge Voltage Source Inverter (HB-VSI), high dc-link capacitances are required. This necessitates the employment of short-lifetime and bulky electrolytic capacitors. In this paper, an analysis for the performance of low dc-link capacitances-based HB-VSI is presented to elucidate its ability to generate an enhanced fundamental output voltage magnitude without increasing the voltage rating of the involved switches. This feature is constrained by the load displacement factor. The introduced enhancement is due to the ac components of the capacitors' voltages. The presented approach can be employed for multi-phase systems through using multi single-phase HB-VSI(s). Mathematical analysis of the proposed approach is presented in this paper. To ensure a successful operation of the proposed approach, a closed loop current controller is examined. An expression for the critical dc-link capacitance, which is the lowest dc-link capacitance that can be employed for unipolar capacitors' voltages, is derived. Finally, simulation and experimental results are presented to validate the proposed claims.

Key words: Enhanced output voltage, Half-bridge voltage source inverter, Low dc-link capacitances

I. INTRODUCTION

CONVENTIONAL two-level Half-Bridge Voltage Source Inverter (HB-VSI), shown in Fig.1a, is one of the most common VSIs which can be used in various applications [1]-[6]. The HB-VSI has a limited ac output voltage magnitude, i.e. voltage buck capability. When sinusoidal pulse width modulation is employed, by varying the peak of the modulating signal (M) from zero to unity, the ac output voltage magnitude varies linearly from zero to half of the dc input voltage ($0.5V_{dc}$). Then by increasing M above unity, a higher output voltage magnitude, but with low order harmonics, is generated (over modulation). Increasing M more saturates the output voltage, and a square waveform with a fundamental output voltage

magnitude of $2V_{dc}/\pi$ is obtained. This represents the maximum achievable value of the fundamental output voltage magnitude in the HB-VSI [7]. If a higher ac output voltage value is required, typically a boosting circuit between the dc source and the dc-link capacitors or a step-up transformer at the output stage can be added [1], [8]. The main drawback of these solutions is adding a further hardware stage, which affects negatively the system cost, efficiency and reliability [9, 10]. On the other hand, Z-source HB-inverter has been proposed in [8, 11] to enhance the fundamental output voltage of the HB-VSI efficiently. Yet, passive elements have to be added.

In HB-VSI, the load current circulates through the two dc-link capacitors, which results in capacitor voltage fluctuations (ac components) generating distorted output voltage [12, 13]. Conventionally, to reduce these fluctuations, large and bulky dc-link electrolytic capacitors, with a short lifetime, are employed. In HB-VSI, the voltage of each capacitor of the dc-link has typically a dc component, an ac component with the fundamental frequency, and insignificant high frequency components which can be neglected. Therefore,
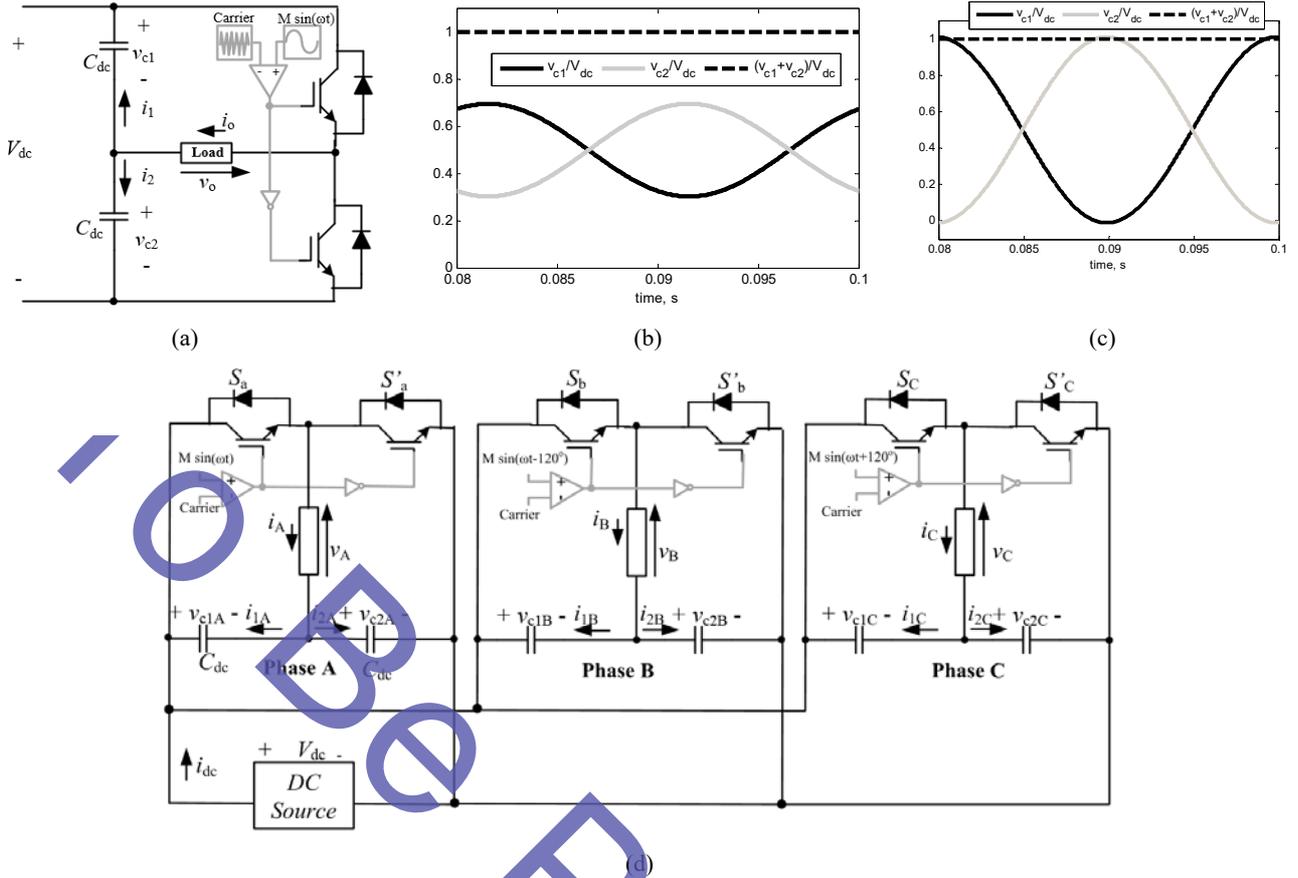
Fig. 1. HB-VSI with low dc-link capacitances (a) single-phase topology, (b) corresponding voltages of the dc-link capacitors at $C_{dc}>C_{cr}$, (c) corresponding voltages of the dc-link capacitors at $C_{dc}=C_{cr}$, and (d) three-phase version of low capacitances HB-VSI.

the dc component and the ac component with the fundamental frequency are only considered throughout this paper.

In this paper, employing low dc-link capacitances with small size, is investigated to enhance the fundamental output voltage magnitude of the HB-VSI. This is constrained to inductive loads, which is the most common ac load. When low dc-link capacitances are employed, the effect of the corresponding ac components of dc-link capacitors' voltages is considerable. These ac components may enhance the fundamental component magnitude of the HB-VSI output voltage (based on the value of the load Displacement Factor (DF) as will be shown in the following sections). Employment of low dc-link capacitances yields a distorted load voltage. Nevertheless, the load current is maintained sinusoidal with the fundamental frequency. Operating with low dc-link capacitances influences positively the system cost and lifetime as non-electrolytic dc-link capacitors can be employed [14], [15]. Mathematical analysis of the proposed approach is presented in this paper for single-phase as well as three-phase systems by employing one and three single-phase HB-VSI(s), respectively.
Moreover, a detailed illustration for designing the dc-link capacitors is presented.

The dc-link capacitances should be properly selected to ensure unipolar voltages across the dc-link capacitors, i.e. their values should be larger than the capacitance at which the peak of ac component of the capacitor voltage reaches $0.5V_{dc}$. For given specifications, a flow chart is presented in this paper to select the proper dc-link capacitances. Finally, simulation and experimental results are presented to validate the proposed approach. The main advantages of the proposed approach can be summarized as follows:

(i) The proposed approach provides an enhanced fundamental output voltage magnitude compared to the high dc-link capacitances-based HB-VSI especially for inductive loads with low DF,

(ii) The proposed approach provides operating with switches rated at the dc input voltage regardless of capacitor voltage fluctuation which affects positively the inverter voltage rating,

(iii) Low dc-link capacitances allows employment of non-electrolytic capacitors which affects positively on the overall cost and lifetime of the inverter.

II. AC COMPONENTS OF HB-VSI DC-LINK CAPACITORS WITH LOW CAPACITANCES

In this section, the analysis of the ac components of

single-phase HB-VSI dc-link capacitors with low capacitances, is presented. This analysis can be extended as well to the multi-phase HB-VSI due its modularity. Based on Fig.1a, using sinusoidal pulse width modulation, a bipolar output voltage (+/-0.5V_{dc}) appears across the load. This results in a sinusoidal load current with harmonic components that depend on the load DF, modulation index and modulation frequency ratio. The load current is divided into two currents, as shown in Fig. 1a, namely (i_1 and i_2) which represent the currents of dc-link capacitors. As the fundamental component of each dc-link capacitor current (i_{1F} or i_{2F}) results in the main ac component of the capacitor voltage ($v_{c1\,AC}$ or $v_{c2\,AC}$), respectively, only the fundamental component of the output current will be considered in the following analysis (i.e. the effect of the harmonic components will be neglected).

The load current (i_o) circulates through the dc-link capacitors (C_{dc}) as shown in Fig.1a. This results in anti-phase ac voltage components across the dc-link capacitors as shown in Fig.1b (assuming inductive load). It is clear that the voltage of each capacitor has two components (dc and ac components). The dc components of the capacitors' voltages equal 0.5V_{dc}, while the phasors of the ac components can be expressed as follows,

$$V_{c1\,AC} = -I_{1F}\left(-j\frac{1}{\omega C_{dc}}\right) \quad (1)$$

$$V_{c2\,AC} = I_{2F}\left(-j\frac{1}{\omega C_{dc}}\right) \quad (2)$$

where $\boldsymbol{I_{1F}}$ and $\boldsymbol{I_{2F}}$ are the fundamental components of the currents i_1 and i_2, respectively, and ω is the angular frequency of the output voltage. The fundamental component of the currents i_1 and i_2 equals $0.5i_{o1}$, where i_{o1} is the fundamental component of the output current.

From (1) and (2), and for a load current with a fundamental component of $i_{o1} = I_m \sin(\omega t + \theta_i)$, the corresponding ac components of the dc-link capacitors' voltages are given by,

$$v_{c1\,AC}(\omega t) = \frac{I_m}{2\omega C_{dc}}\sin\left(\omega t + \theta_i + \frac{\pi}{2}\right) \quad (3)$$

$$v_{c2\,AC}(\omega t) = \frac{I_m}{2\omega C_{dc}}\sin\left(\omega t + \theta_i - \frac{\pi}{2}\right) \quad (4)$$

where I_m is the peak of the fundamental output current component, and θ_i is the phase angle of the load current. Based on (3) and (4), it is clear that:

(i) The two components are anti-phase and their summation equals zero, i.e. $v_{c1} + v_{c2} = V_{dc}$ as shown in Fig.1b. This means that the voltage ratings of the involved switches are not influenced by the fluctuation of the capacitors' voltages.

(ii) The peak of the dc-link capacitors' voltages ac components can be expressed by,

$$V_{ci\,AC} = \frac{I_m}{2\omega C_{dc}} \quad (5)$$

i.e., the ac component peak of the capacitor voltage mainly

depends on the peak of the fundamental component of the load current, dc-link capacitance (C_{dc}), and the angular frequency of the load voltage.

To have a unipolar voltage across each of the dc-link capacitors, the peak of the dc-link capacitors' voltages ac component should be lower than 0.5V_{dc}, i.e.

$$C_{cr} = \frac{I_m}{\omega V_{dc}} \quad (6)$$

where C_{cr} is the critical capacitance which is defined as the lowest dc-link capacitance that can be employed for unipolar capacitor voltages. The corresponding voltage fluctuations of the dc-link capacitors at the critical value of the dc-link capacitances are shown in Fig.1c assuming inductive load (i.e. ac component peak equals 0.5V_{dc}).

The three-phase version of the low dc-link capacitances based HB-VSI is shown in Fig. 1d, which consists of three single-phase HB-VSI. The three-phase version can be used in three-phase motor drive systems with open winding motors. Also, it can be used for integrating photovoltaic systems with the three-phase electric power grid through an open winding transformer.

III. OPERATION OF HB-VSI FEEDING AN INDUCTIVE LOAD WITH ENHANCED OUTPUT VOLTAGE MAGNITUDE

In this section, the operation and analysis of the HB-VSI, feeding an inductive load with enhanced output fundamental voltage, are presented.

A. Mathematical Analysis

Assume the following conditions,

- Modulating signal =$M \sin(\omega t)$, where $0 \le M \le 1$.
- Load impedance (inductive load) = $Z\angle\varphi$.
- $v_{o1} = V_{o1}\sin(\omega t + \theta)$, where v_{o1} is the fundamental component of the output voltage, and V_{o1} and θ are its magnitude and phase angle (which depends on the operational conditions), respectively. The expressions for the fundamental output voltage magnitude and phase angle will be found in the following analysis.
- The ac component of the capacitor voltage depends on the fundamental ac current that passes through the capacitor which is $0.5i_{o1}$, i.e. the corresponding ac component can be expressed by,

$$\boldsymbol{V}_{c1\,AC} = 0.5\frac{V_{o1}}{\omega C_{dc}Z}\angle\left(\theta - \varphi + \frac{\pi}{2}\right) \quad (7)$$

This component impacts the load voltage shape, i.e. the fluctuation appears on the load voltage as shown in Fig.2a, assuming 3 kHz switching frequency. On the other hand, if high dc-link capacitances are employed, the load voltage will be as shown in Figs. 2b, assuming 3 kHz switching frequency.

Based on Figs. 2c and 2e, the output voltage at low C_{dc} can be expressed as a summation of two terms as in (8). The first term ($0.5MV_{dc}\angle 0$) represents the output voltage when high dc-link capacitances are employed, while the second term
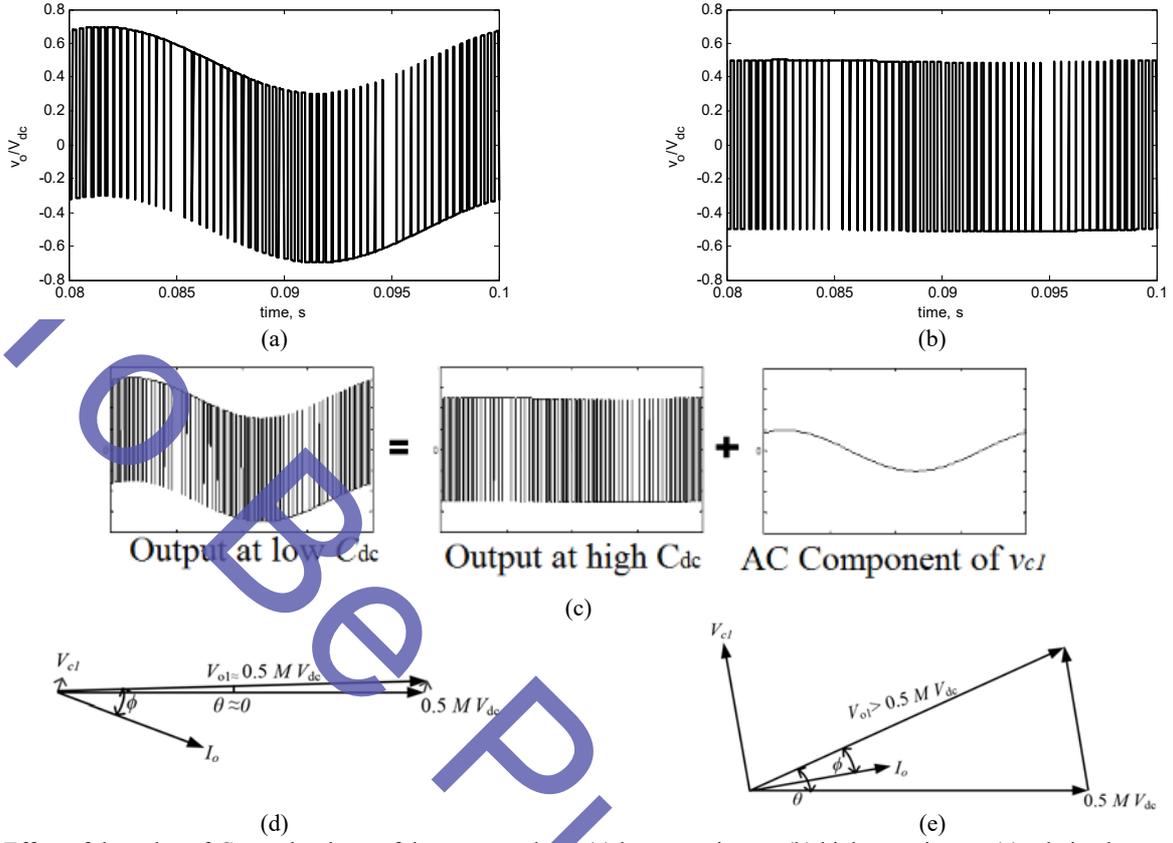

Fig. 2. Effect of the value of C_{dc} on the shape of the output voltage (a) low capacitance, (b) high capacitance, (c) relation between the output voltages at low and high dc-link capacitances, (d) phasor diagram in case of high dc-link capacitances and (e) phasor diagram in case of low dc-link capacitances .

represents the ac component of the upper dc-link capacitor ($v_{c1\,AC}$).

$$V_{o1}\angle\theta = 0.5MV_{dc}\angle 0 + 0.5\frac{V_{o1}}{\omega C_{dc}Z}\angle\left(\theta - \varphi + \frac{\pi}{2}\right) \quad (8)$$

Equation (8) can be re-written as follows,

$$V_{o1}\angle\theta = 0.5MV_{dc} + 0.5\frac{V_{o1}}{\omega C_{dc}Z}\left(\cos\left(\theta - \varphi + \frac{\pi}{2}\right) + j\sin\left(\theta - \varphi + \frac{\pi}{2}\right)\right) \quad (9)$$

i.e.,

$$\begin{aligned} V_{o1}\cos\theta + j\,V_{o1}\sin\theta \\ = 0.5MV_{dc} \\ + 0.5\frac{V_{o1}}{\omega C_{dc}Z}(-\sin(\theta - \varphi) \\ + j\cos(\theta - \varphi)) \end{aligned} \quad (10)$$

By equating the real and imaginary terms, the following equations can be extracted,

$$V_{o1}\left(\cos\theta + \frac{1}{2\omega C_{dc}Z}\sin(\theta - \varphi)\right) = 0.5MV_{dc} \quad (11)$$

$$\sin\theta = \frac{1}{2\omega C_{dc}Z}\cos(\theta - \varphi) \quad (12)$$

For a given input dc voltage, peak of modulating signal, load impedance, and dc-link capacitances, equation (12) can be used to obtain the value of θ, then substituting in (11), the value of V_{o1} can be obtained. For a given operational data, the dc-link capacitances should be selected higher than the critical capacitance to ensure unipolar capacitor voltages. The critical capacitance can be expressed as a function of the fundamental output voltage magnitude as follows,

$$C_{cr} = \frac{V_{o1}}{\omega Z V_{dc}} \quad (13)$$

As V_{o1} depends on the selected value of dc-link capacitances, the flow chart that can be used to select the dc-link capacitance is presented as shown in Fig.3.

B. Numerical Example

Based on the aforementioned mathematical relations and for $M = 1$, $\omega = 100\pi$ rad/s, $V_{dc} = 100$V, $Z = 5\Omega$, $\phi = 45^{\circ}$, and $C_{dc} = 1$mF;

The corresponding V_{o1} equals 62V. It is clear that the output voltage magnitude>50V, where 50V represents the fundamental output voltage magnitude in case of HB-VSI with high dc-link capacitances. So the corresponding enhancement of the fundamental output voltage magnitude equals 24% in the presented case. The corresponding C_{cr} equals 0.4 mF (i.e., $C_{dc} > C_{cr}$). While, the corresponding θ equals 16.2º. Finally, the peak of ac component of the capacitor voltage equals 19.7V.


(b)

Fig. 4. Simulation results of the given numerical example. (a) voltages of the dc-link capacitors and their summation and (b) actual and filtered output voltage.

To validate the aforementioned calculation, a simulation model has been built for a single-phase HB-VSI with the aforementioned specifications, and the corresponding

Fig. 3. Flowchart to select proper dc-link capacitances.
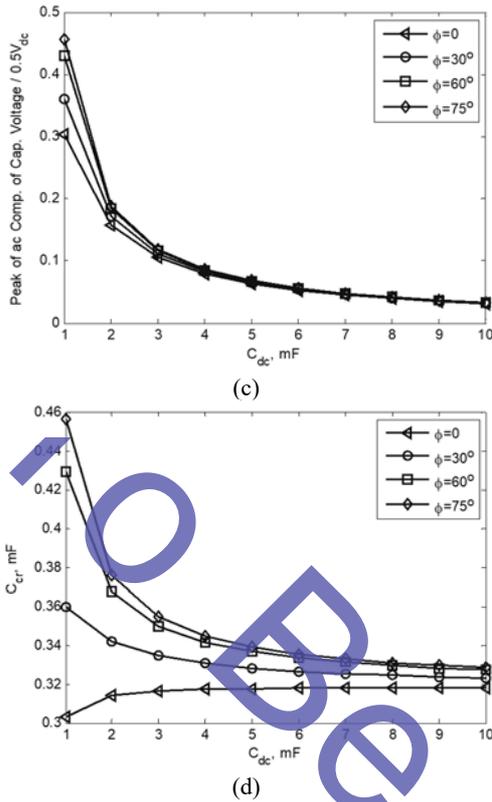

(a)

(a)

(b)

(c)

(d)
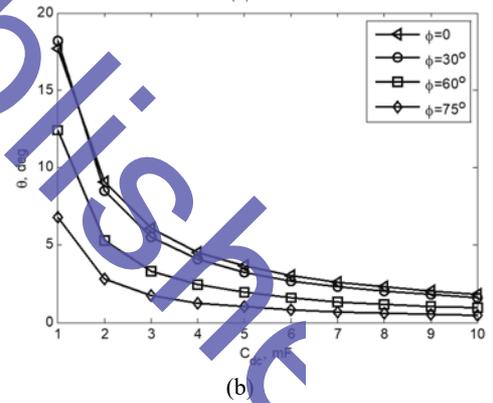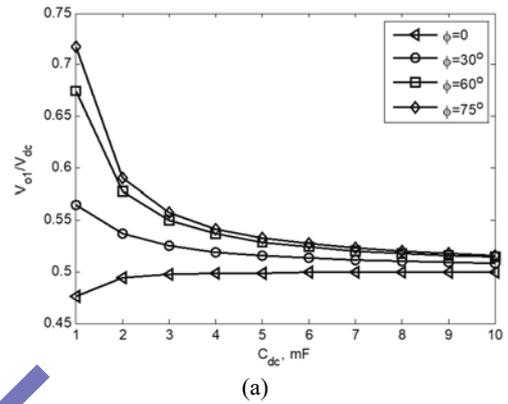
Fig. 5. Effect of dc-link capacitance and lagging load DF on the enhancement of the fundamental output voltage magnitude and other system variables for M=1, V_{dc}=100 V, and Z=5 Ω at 50 Hz. (a) V_{o1}/V_{dc} versus dc-link capacitance, (b) θ versus dc-link capacitance, (c) peak of ac component/$0.5V_{dc}$ versus dc-link capacitance, and (d) critical capacitance versus dc-link capacitance.
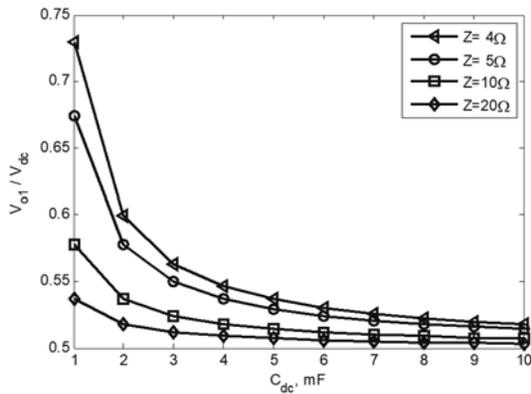

Fig. 6. Effect of load impedance magnitude on V_{o1} at 0.5 lagging load DF and different values of dc-link capacitances.

simulation results are shown in Fig. 4 assuming 3 kHz switching frequency. Based on Fig. 4, it is clear that the simulation results are identical to the calculated values.

C. Effect of dc-link Capacitance and Load on the Fundamental Output Voltage Magnitude

In this section, the effect of the dc-link capacitances and

load on the enhancement of the fundamental output voltage magnitude is presented.

Based on the aforementioned equations, and for V_{dc} = 100V, M = 1, Z = 5Ω (inductive load) and ω=100π rad/s, the variation of peak of the fundamental output voltage, phase angle of the fundamental output voltage, and the peak of ac component of the capacitor voltage with the variation of the dc-link capacitance (C_{dc}) for different load DFs are shown in Figs. 5a-5c.

Based on (13), the corresponding critical capacitances for different cases are shown in Fig. 5d. It is clear that enhanced output voltage magnitude increases with the decreasing of dc-link capacitances. It is also clear that the dc-link capacitance is higher than the critical capacitance in all cases (Fig.5d) to ensure unipolar capacitor voltage.

On the other hand, Fig. 6 shows the effect of load impedance magnitude on the enhancement of the fundamental output voltage magnitude at 0.5 lagging load DF. Based on the results shown in Figs. 5 and 6, the following points can be concluded:

(i) It is clear from Fig.5a that there is a limited or no enhancement for the fundamental output voltage magnitude in case of load with high lagging load DFs. The main reason for that is the phase angle and the magnitude of the fundamental ac component of the capacitor voltage which mainly depend on the load angle as shown in Fig. 7. The actual and filtered output voltage at unity load DF and 0.5 lagging load DF are shown in Figs. 7a and 7b respectively.

(ii) Based on Fig. 5, for a relatively low and lagging load DFs, as dc-link capacitance decreases (but still above the critical value), the peak of fundamental output voltage
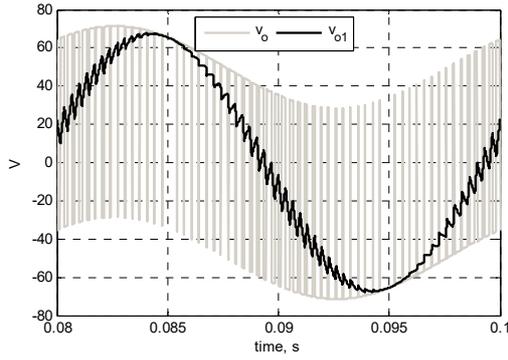

(a)
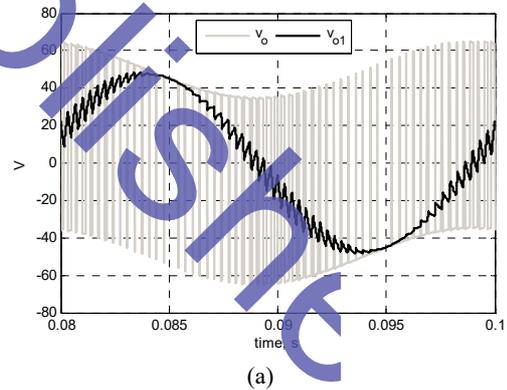
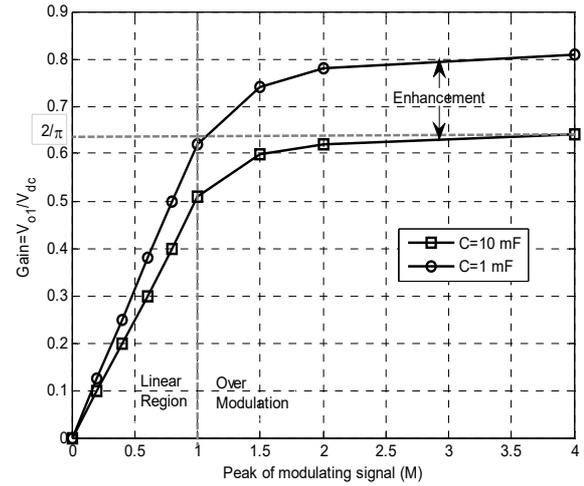Fig. 7. Actual and filtered output voltage at different load DFs (a) unity DF, (b) 0.5 lagging DF.

Fig. 8. Gain versus M for different values of dc-link capacitance (C_{dc}) assuming an input dc voltage of 100 V, and Z=5 Ω, load angle ϕ=45º at 50 Hz.

increases, i.e. the proposed approach is more beneficial when feeding loads with low lagging load DFs

(iii) Based on Fig.6, as the load impedance magnitude increases, the enhancement in the fundamental output voltage magnitude decreases because the load current decreases, which results in decreasing the ac component of dc-link capacitor voltage.
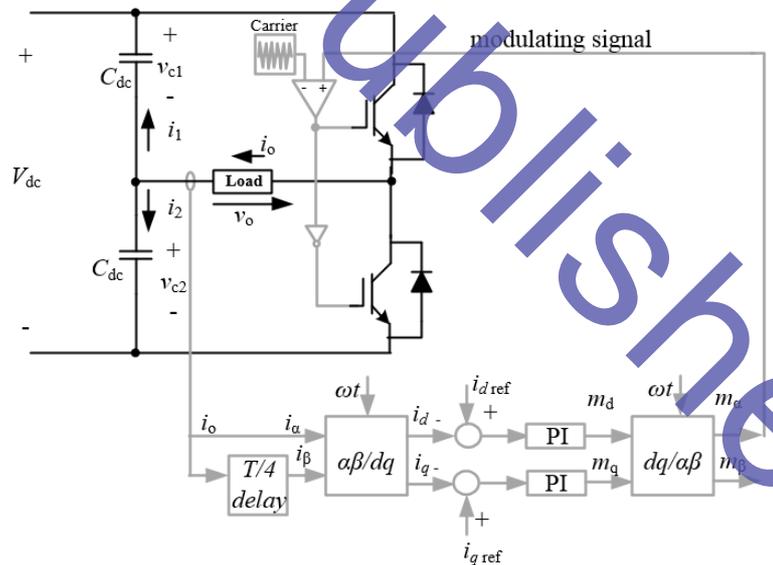

Fig. 9. The per-phase current controller of the proposed approach

D. Assessment of the HB-VSI with Low dc-link Capacitances.

In this subsection, the low dc-link capacitances based HB-VSI is compared with the high dc-link capacitances

based HB-VSI in terms of (i) gain versus M, and (ii) voltage rating of the involved switches. In this assessment, a simulation model has been built for the HB-VSI with input dc voltage of 100V, and Z= 5Ω, ϕ = 45º at 50Hz. This model has been run multi-times to check the variation of the fundamental output voltage peak (V_{o1}) with the variation of

(*M*) for two different cases (C_{dc} =10 mF, and C_{dc}=1 mF). The corresponding result is shown in Fig.8.

With respect to the relation between gain and *M* and based on Fig.8, it is clear that;

(i) Both relations have linear region till *M*=1, then they go into saturation region (i.e., over modulation effect).

(ii) Higher voltage can be obtained from the HB-VSI with lower dc-link capacitance (i.e. operation with enhanced fundamental output voltage magnitude), as the output voltage enhancement is clearly shown in Fig. 8.

With respect to the voltage rating of the involved switches in both cases, based on Fig.8, for V_{o1}=70V and *M*=1; the required input dc voltage in each case can be estimated as follows;

(i) In case of high dc-link capacitances (C_{dc}=10 mF), at *M*=1, the gain equals 0.52, i.e. for V_{o1}=70V, the suitable V_{dc} is 135 V.

(ii) In case of low dc-link capacitances (C_{dc}=1 mF), at *M*=1, the gain equals 0.63, i.e. for V_{o1}=70V, the suitable V_{dc} is 110 V.

As the involved switches are rated at the input dc voltage, the switches in the case of low dc-link capacitances will

have a lower voltage rating for the same output voltage which affects positively on the converter cost. On the other hand, with respect to the efficiency, the conduction losses (P_c) and switching losses (P_{sw}) of the HB-VSI leg are given by (14) and (15) respectively [16],
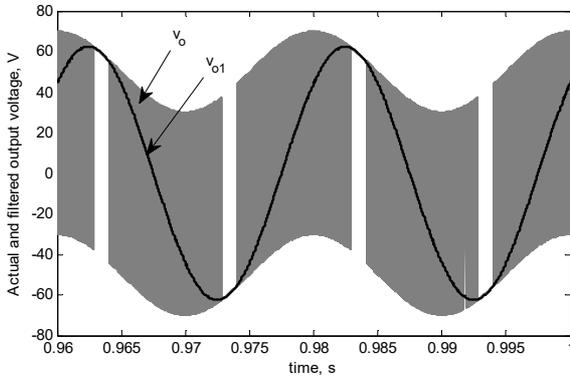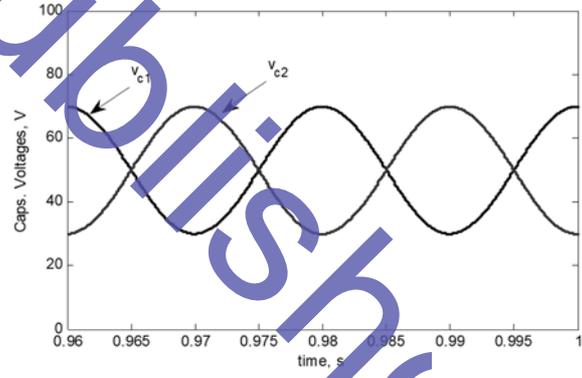
$$P_c \cong \left(\frac{V_{TO} + V_{DO}}{\pi}\right) I_m + \left(\frac{R_{TO} + R_{DO}}{4}\right) I_m^2 \qquad (14)$$

$$P_{sw} = \frac{2}{\pi} f_{sw}(t_{on} + t_{off})V_{DC}\, I_m \qquad (15)$$

where V_{T0} and R_{T0} are the on-state voltage and resistance of the IGBTs, V_{D0} and R_{D0} are the on-state voltage and resistance of the anti-parallel diodes, I_m is the peak of module output current, f_{sw} is the switching frequency, t_{on} is the IGBT turn-on, t_{off} is the IGBT turn-off time, and V_{DC} is the input dc-link voltage. Based on (14), if the load current magnitude (I_m) is controlled to be constant at a certain level in both cases (low and high dc-link capacitances) and identical switches with the same on-state voltage and resistance are employed, the conduction losses in both cases will be the same. On the other hand, based on (15), the switching losses in case of low dc-link capacitance HB-VSI will be lower since the HB-VSI with low dc-link capacitances needs lower dc-link voltage to generate the same output current peak, i.e. it will offer higher efficiency.

IV. CLOSED LOOP CURRENT CONTROLLER FOR THE PROPOSED APPROACH

In this section, the presented approach is assessed through closed loop operation. Fig. 9 shows the per-phase current controller of the proposed approach, where *T* is the periodic time of output voltage and current. The per-phase current controller is responsible for maintaining the direct and
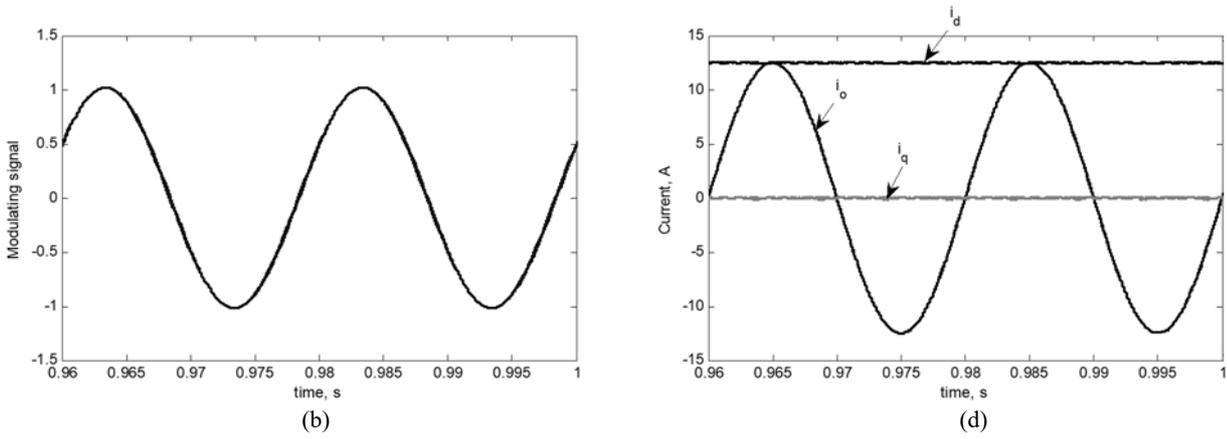

(a)

(c)

(b)

(d)

Fig. 10 Performance of the per-phase closed loop current controller for the presented numerical example (a) output voltage, (b) output current, (c) modulating signals, and (d) voltages of dc-link capacitors

quadrature current components within the desired levels. The current controller of the proposed approach is based on the conventional Proportional-Integral (PI) based current controller for single-phase systems. In the presented current controller, the phase current is measured and transformed into dq components (i_d and i_q). Then the reference of direct and quadrature components ($i_{d\,ref}$ and $i_{q\,ref}$) compared with their actual values (i_d and i_q), and the error signals are fed to the PI controllers. The outputs of PI controllers are the reference direct and quadrature components of the modulating signal (m_d and m_q) which can be transformed into αβ components (m_α and m_β). The α-component (m_α) represents the reference modulating signal for the involved HB-VSI. Finally, the generated modulating signal is used to generate the gate pulses of this phase switches by employing sinusoidal pulse width modulation. In three-phase systems, this current controller should be applied to the other phases with the same concept, but shifted by -120º and +120º.

To show the performance of the per-phase controller, Fig.10 shows the variation of output voltage, output current, modulating signal, and voltages of dc-link capacitors assuming the following parameters: (V_{dc} = 100V, C= 1mF, Z = 5Ω, ϕ= 45º, ω = 100π rad/s, 10 kHz carrier signal, $i_{d\,ref}$ = 12.5A, $i_{q\,ref}$ = 0 A, and PI constants of k_p = 0.2 and k_i = 2). It is
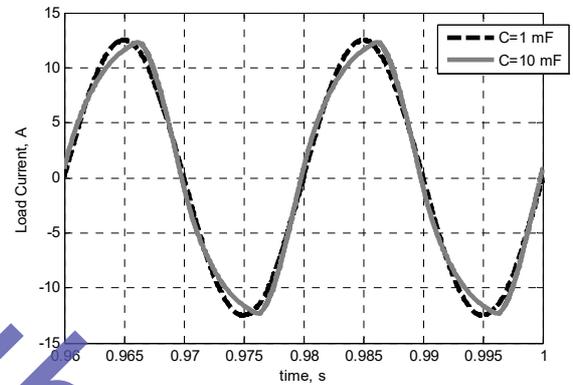

Fig. 11. Comparison between the output current at low and high dc-link capacitance HB-VSIs for the presented numerical example.

clear that enhanced output current with good quality is generated with the low-dc link-based HB-VSI at unity peak modulating signal.

It has to be noted that in case of high dc-link capacitances HB-VSI, the unity peak modulating signals is able to generate sinusoidal current of 10 A with good quality, i.e. 25% enhancement is achieved with employing low-dc link capacitances assuming a unity peak modulating signal in both cases. To generate the same fundamental component (12.5A)
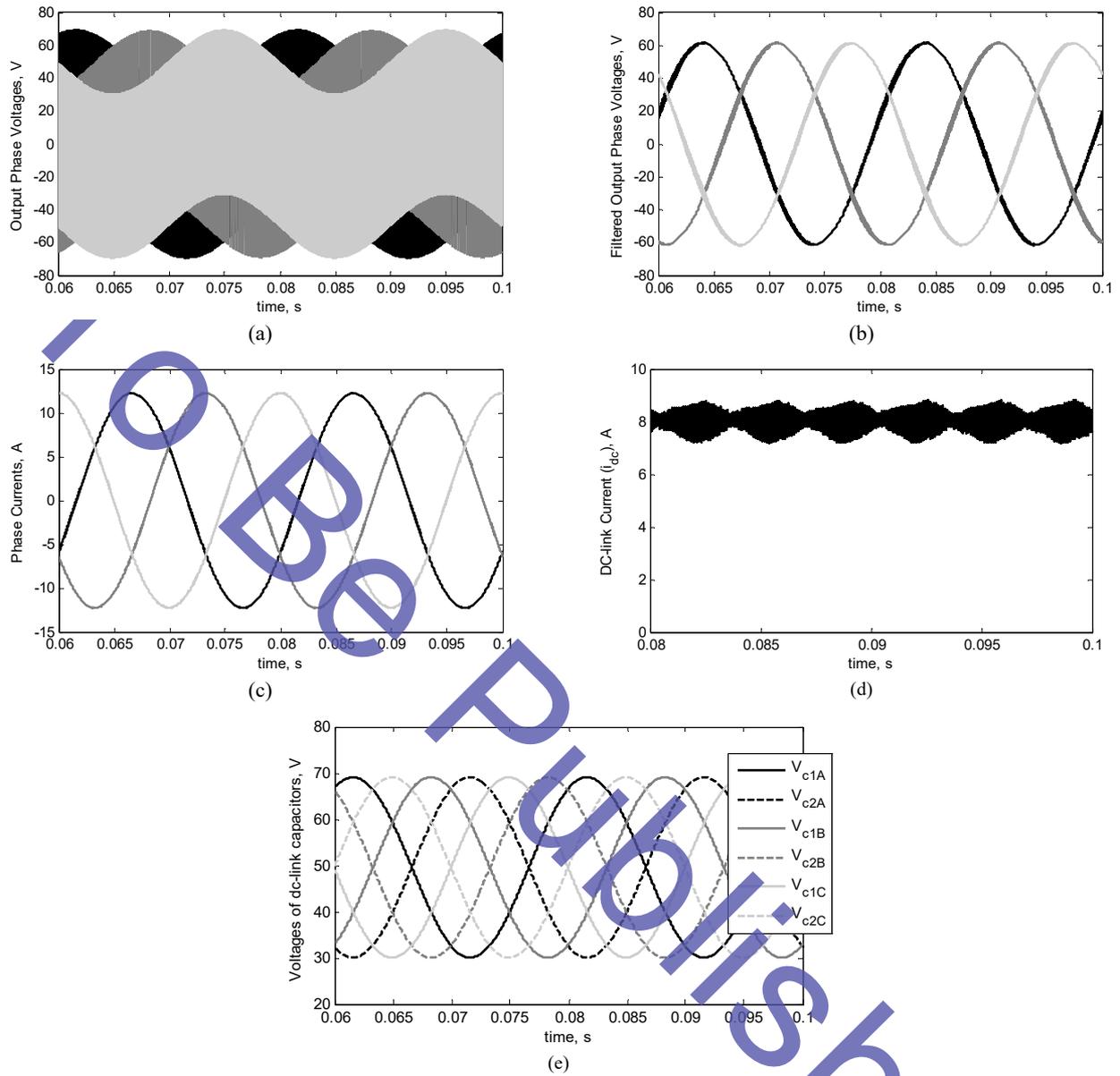
Fig. 12. Simulation results for three-phase load (a) actual output voltages, (b) filtered output voltages, (c) phase currents, (d) dc current, and (e) voltages of the dc-link capacitors.

TABLE I
Simulation Parameters

DC input voltage, V_{dc}	100 V series with 0.2 Ω
No. of dc-link capacitors	6 (2 per each phase)
DC-link capacitance (C_{dc})	1 mF
Load impedance at 50 Hz	5∟45° per phase
Carrier frequency	10 kHz

in case of high-dc link capacitances (10 mF) HB-VSI, the inverter should be operated in the over modulation region,

hence a distorted output current is generated as shown in Fig.11.

The THD of the load current in case of low and high capacitance in case of fundamental peak of 12.5A equals 0.45% and 8.87% respectively.

V. SIMULATION OF THREE PHASE HB-VSI

A simulation model has been built for three-phase HB-VSI (shown in Fig.1d) to show the performance of three-phase HB-VSI with low dc-link capacitances. The

simulation parameters are given in Table I.

A. Open loop control

Firstly, the performance of the proposed approach has
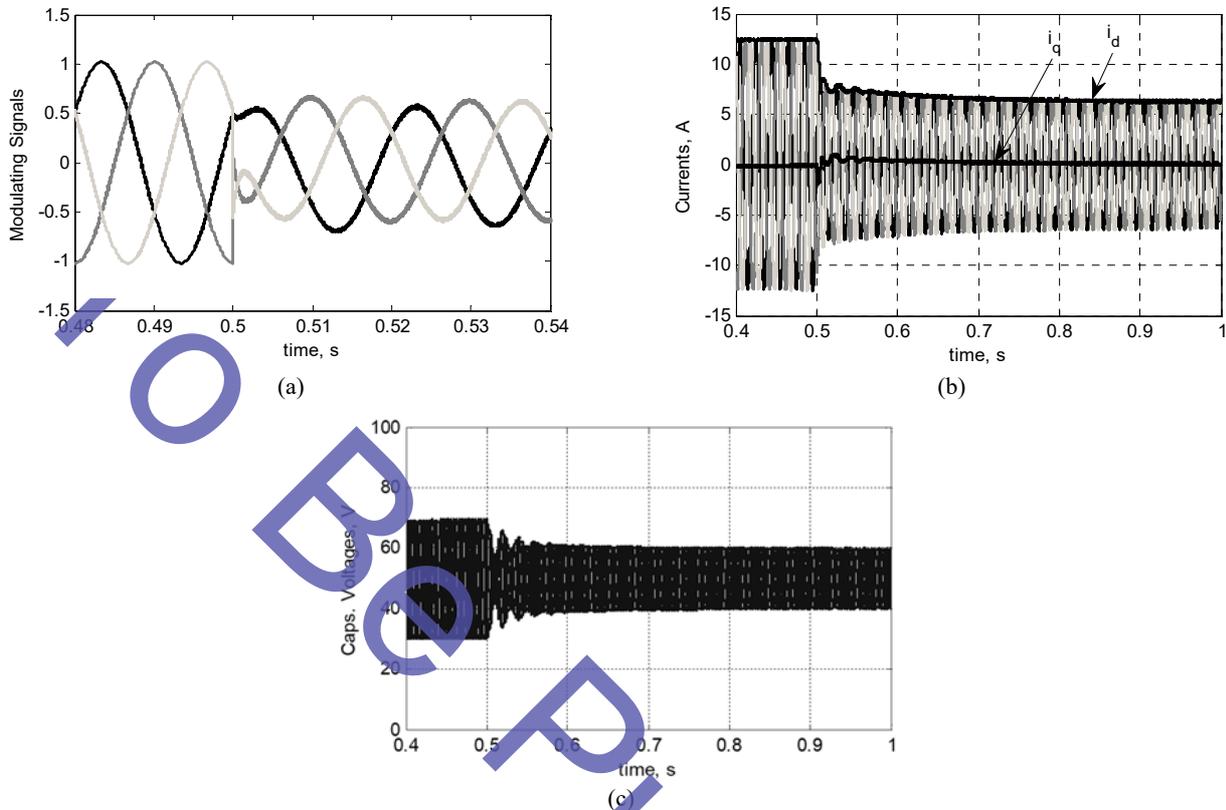

(a)

(b)

(c)

Fig.13. Simulation results for the closed loop controller testing. (a) Modulating signals, (b) load currents, and (c) capacitors' voltages.

been tested using unity peak three-phase modulating signals. The corresponding simulation results are shown in Fig. 12. Figs. 12a and 12b show the actual and filtered output voltages. It is clear that there is an enhancement of the fundamental output voltage magnitude (24% in the presented case) compared to the high dc-link capacitances based HB-VSI.

Fig.12c shows the phase currents, as the currents are pure sinusoidal and there is no effect from the capacitor voltage fluctuation on the quality of the output currents. Fig.12d shows the current at the dc side (i_{dc} in Fig.1d). It is clear that a constant current is drawn from dc source, which is an important issue in some application such as PV and fuel cell applications. Finally, Fig.12e shows the voltages of dc-link capacitors. It is clear that the ac components of the dc-link capacitors in each phase are anti-phase, so the summation of the voltages of the dc-link capacitors of each phase equals the input dc voltage (V_{dc}), i.e. voltage enhancement is achieved without increasing the voltage rating of the involved switches.

B. Closed loop control

In this subsection the performance of the proposed closed loop current controller is tested by varying the direct current reference from 12.5A to 6.25A at t=0.5s, assuming zero quadrature current component. The corresponding simulation results are shown in Fig. 13.
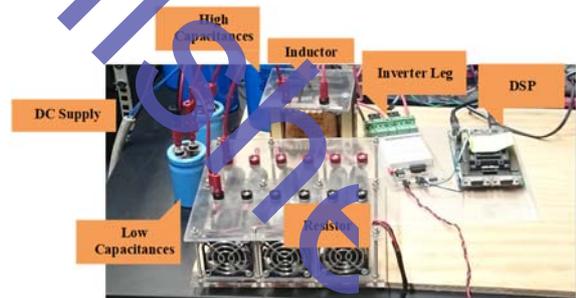

Fig. 14. Experimental setup.

Fig. 13a shows the variation of three-phase modulating signals with the operation, while Fig.13b shows the three-phase load currents and their per-phase direct and quadrature components. Finally, the corresponding capacitors' voltages are shown in Fig.13c.

It is clear that the voltage fluctuations decrease with the decrease of current magnitude. Based on the presented results,

the proposed controller is able to track the current reference successfully.

VI. Experimental Validation

A simple single-phase HB-VSI has been used for experimental verification (Fig. 14) with the parameters shown in Table II. Two values of dc-link capacitance (Cdc) have

Fig. 15. Experimental results for low dc-link capacitance case. (a) voltages of the dc-link capacitor, (b) load voltage, (c) the load current , and (d) FFT for the load current.
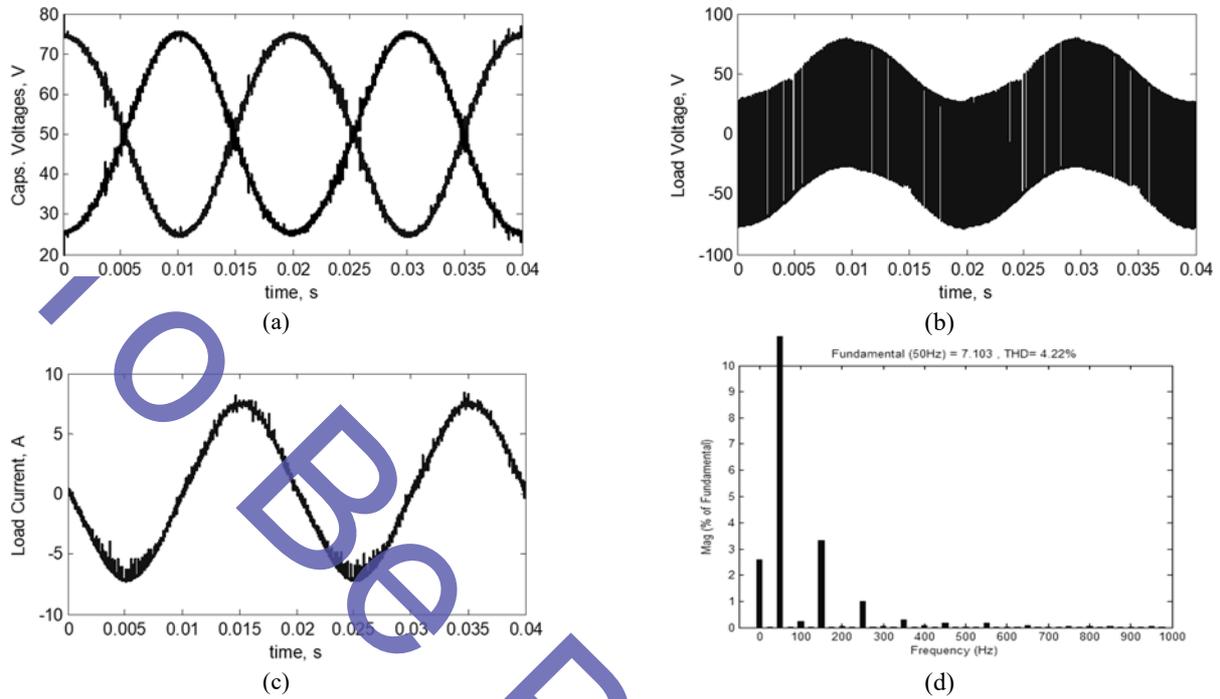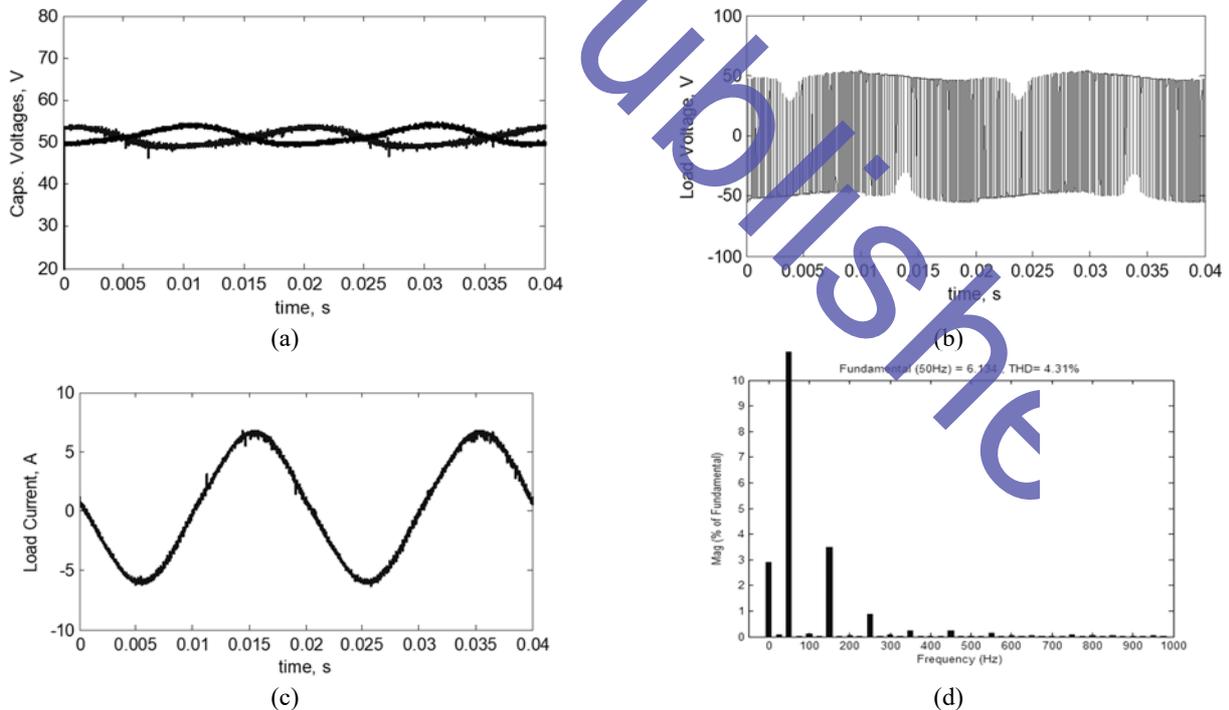

Fig. 16. Experimental results for high dc-link capacitance case. (a) voltages of the dc-link capacitor, (b) load voltage, (c) the load current , and (d) FFT for the load current.

been considered 450µF and 4700µF to show the difference

between the low and high dc-link capacitances.

A. Open loop control

In this mode, a modulating signal with unity peak is applied.

The corresponding experimental results for low and high dc-link capacitances along with FFT for the load currents are shown in Figs. 15 and 16 respectively.

It has to be noted that both values are greater than the critical capacitance, i.e. the peak of ac component of the capacitor

TABLE II
Experimental Setup Parameters

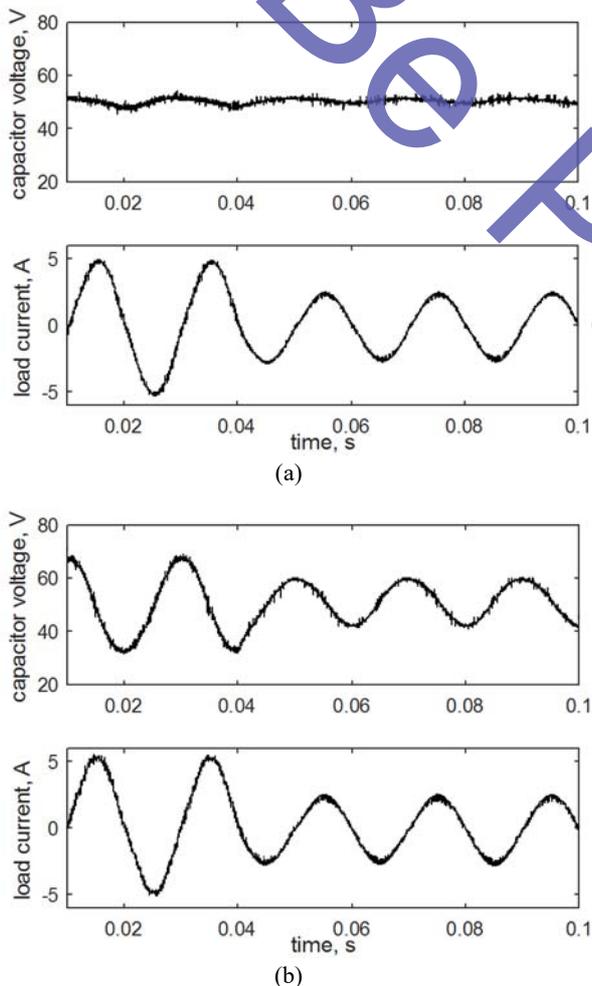| Input dc voltage, V_{dc}	100 V
Load (RL inductive load)	R=6 Ω, and L=10mH
Frequency of the Carrier	5 kHz
Modulating signal (open loop)	1 sin (100π t)
DC-link capacitances	Case 1: 450µF, Case 2: 4700µF

(a)

(b)

Fig.17. Experimental results for the closed loop control (a) high dc-link capacitances case, (b) low dc-link capacitances case.

voltage is less than $0.5V_{dc}$). The flow chart shown in Fig. 3 can be used to check that the selected values are greater than the critical capacitance value. Figs.15a and 16a shows the variation of the voltages of dc-link capacitances. It is clear that the ac components of capacitors' voltages are anti-phase and their summation equals zero. Fig. 15c and 16c sows the load currents, it is also clear that the load currents in both cases are sinusoidal.

The current spikes (high frequency pulsating current) shown in the load currents (Figs. 15c and 16c) are due to device switching as high dv/dt and di/dt are the major sources of EMI noise with the existence of parasitic elements such as dc-link capacitor series inductance, and circuit stray capacitances/inductances [17]. As the current in the case of low dc-link capacitances is higher, a higher noise is expected with the switching. The FFT for the load current in case is shown in Figs.15d and 16d respectively.

Based of Figs. 15d and 16d, it is clear that both currents have almost the same THD. On the other hand, the magnitude of fundamental load current in case of low dc-link capacitances based HB-VSI is 7.1 A which is greater than its value in case of high dc-link capacitances based HB-VSI (6.134 A). This confirms the enhancement of the fundamental output voltage magnitude with the low dc-link capacitances based HB-VSI. The enhancement of the fundamental output voltage magnitude in the presented experimental results is 15.7%.

B. Closed loop control

The performance of the HB-VSI with low and high dc-link capacitances is investigated when the closed loop controller (shown in Fig.9) is applied. A step reference is defined for the ac output current peak (step change from 5A to 2.5A) with PI constants of k_p=0.2 and k_i=8. The corresponding simulation results for the high and low dc-link capacitances are shown in Figs. 17a and 17b, respectively. It is clear that; (i) the ac output current is generated as desired successfully in both cases, and (ii) the voltage fluctuations decrease with the decrease of current magnitude.

VII. CONCLUSION

In this paper, the performance of the low dc-link capacitances based HB-VSI has been presented. The main advantages of the proposed approach are:

(i) Enhanced fundamental output voltage magnitude compared to the high dc-link capacitances based HB-VSI when feeding an inductive load (especially at low load DF),

(ii) Operating with switches rated at the dc input voltage regardless of capacitor voltage fluctuation which influences positively on the inverter cost and efficiency compared to the high dc-link capacitances based HB-VSI assuming the same fundamental output voltage magnitude, and

(iii) Operating with low dc-link capacitances allows the employment of non-electrolytic capacitors which impacts positively on the overall cost and lifetime.

A detailed mathematical analysis of the proposed approach has been presented along with its closed loop current controller. To ensure unipolar capacitor voltage, the selected dc-link capacitor should be greater than the critical capacitance. A flow chart, which can be used to check if the selected dc-link capacitance is suitable or not, has been presented as well. Moreover, a family of curves describing the relation between system variables have been also presented in this paper. Simulation results have been presented to show the viability of the proposed approach in three-phase systems. Finally, experimental validation using single-phase HB-VSI has been made to show the possible enhancement in the output voltage magnitude when low dc-link capacitances are employed.

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