# Bridgeless Buck PFC Rectifier with Improved Power Factor

Mahdi Malekanehrad* and Ehsan Adib†

*,†Department of Electrical and Computer Engineering, Isfahan University of Technology, Isfahan, Iran



**Abstract**

Buck power factor correction (PFC) converters, compared with conventional boost PFC converters, exhibit high efficiency performance in the entire range of universal line voltage. This feature has gotten more attention for eliminating the zero crossing dead angle of buck PFC rectifiers. Furthermore, bridgeless structures for the reduction of conduction losses have been proposed. The aim of this paper is to introduce a single-phase buck rectifier that simultaneously has unity power factor (PF) and bridgeless structure while operating in the continuous conduction mode (CCM). For this purpose, two auxiliary flyback converters without any active switches are applied to a bridgeless buck rectifier to eliminate the zero crossing dead angle and achieve unity power factor, low total harmonic distortion (THD) and high efficiency. The operation and design considerations of the proposed rectifier are verified on a 150W, 48V prototype using a conventional peak-current-mode control. The measurement results show that the proposed rectifier has nearly unity power factor, THD less than 7% and high efficiency.

**Key words:** Bridgeless AC-DC converters, Buck converter, Power factor correction, Zero crossing distortion

## I. INTRODUCTION

The use of power factor correction (PFC) converters as a current shaper in the front stage of ac/dc rectifiers is an effective method to provide high power factor (PF) and low total harmonic distortion (THD) for meeting IEC61000-3-2 [1]. On the other hand, high efficiency is a vital requirement of performance. Meeting the requirements of both high PF and efficiency poses a major challenge for ac/dc rectifiers. Boost converters are the most commonly used PFC converters. However, in universal-line application, the efficiency of a boost PFC is reduced about 1-3% at low-line voltage compared to high-line voltage due to its large operating duty cycle for providing a high voltage gain [2]-[4]. Furthermore, its high output voltage (380-400 V) increases the switch voltage stress and the voltage stress of the second stage switches and reduces efficiency [3], [4].

Recently, the use of front stage buck PFC converter has increased [2]-[25]. According to the authors of [3], a buck PFC converter with 80 VDC output demonstrates high efficiency across the universal-line range. Furthermore, the low output voltage of the buck PFC reduces the voltage stress of the output stage switches and improves the light load performance. In [4], a bridgeless buck PFC was proposed to reduce conduction losses by minimizing the number of simultaneously conducting semiconductor devices. However, in a buck converter, compared to its boost counterpart, there is an inherent dead angle in the input current around the zero crossings of the line voltage for input voltages that are lower than the output. This leads to a high current distortion and a low PF that limits the maximum power level. For example, in [4], the measured PF and THD at full load (700 W) and 115 Vac line voltage are 0.88 and 43.4% and at 10% load (75 W) and 230 Vac they are 0.66 and 19.4%, respectively. Although these values are in compliance with IEC 61000-3-2, the higher losses and EMI due to increased input current peak are drawbacks.

In [21]-[24], for $V_{in}<V_{out}$, an auxiliary flyback converter with an auxiliary switch, diode and inductor is activated to shape the input current and reduce the zero crossing dead angle. However, in these topologies, three or four simultaneously conducting semiconductor devices increase the conduction losses. Due to transition from flyback to buck mode at $V_{in} = V_{out}$, the input current can change abruptly and increase the THD.

In [25], the output capacitor of an auxiliary flyback converter is in series with the switch of a conventional buck converter. Thus, the voltage of the flyback output capacitor is added to the rectified line voltage. As a result, the zero crossing dead angle of the input current is omitted. However, three simultaneously conducting active components in the conducting period of the buck switch increase the conduction losses and reduce the efficiency.

In this paper, a bridgeless unity PF buck rectifier is proposed. Two auxiliary flyback converters are used in a bridgeless buck topology to omit the zero crossing dead angles of the positive and negative half-line cycles. Thus, the proposed rectifier provides both high PF and efficiency. Without any auxiliary switches and only with one auxiliary diode, one low voltage small capacitor and an additional winding on the core of the buck inductor, the dead angle of the input current is omitted and a unity PF is achieved. The operation of the proposed rectifier is verified using a 150 W, 48 V experimental prototype operating in the continuous conduction mode (CCM) using peak-current-mode control method.

## II. Principle of Operation

The proposed bridgeless unity PF buck rectifier is shown in Fig. 1. Figs. 2a and 2b show the operation of the rectifier in the positive and negative half-line cycles, respectively. Due to their similarity, only the positive half-line cycle is described. The buck converter of the positive half-line cycle, consists of a unidirectional switch implemented by diode $D_1$ and switch $S_1$, freewheeling diode $D_5$, filter inductor $L_1$, and output capacitor $C_1$. The auxiliary flyback converter consists of diode $D_3$, small capacitor $C_{a1}$ and inductor $L_3$ that is couple with its buck counterpart $L_1$ with a unity turn ratio. The operation of the rectifier is presented using theoretical waveforms (Fig. 3) and the following assumptions.

- All of the components are ideal except for the coupled inductors $L_{1,3}$ and $L_{2,4}$, where their leakage inductances are included.
- The output capacitors $C_{1,2}$ are large enough to obtain constant output voltages $V_{O1,2}$ in a switching cycle.
- The initial voltage of $C_{a1}$ is equal to $V_{O1}$ ($V_{Ca1}$ ($t_0$) = $V_{O1}$).

*Mode 1* ($t_0$-$t_1$): According to Fig. 4a, by turning the buck switch $S_1$ on, the voltage $V_{ac}$+$V_{Ca1}$-$V_{O1}$ is applied to the buck inductor $L_1$ and $i_{L1}$ increases linearly. The buck inductor current $i_{L1}$ discharges the capacitor $C_{a1}$ and decreases its voltage $V_{Ca1}$ from the initial value $V_{Ca1}$ ($t_0$) =$V_{O1}$ to $V_{O1}$ - $\Delta V_{Ca1}$. The low voltage ripple of $\Delta V_{Ca1}$ is desirable because the line voltage $V_{ac}$ is applied to the inductor $L_1$ and the dead angle of the line current is omitted. The current $i_{L1}$ is increased with a slope of $V_{ac}/L_1$ . At $t = t_1 = DT$, switch $S_1$ is turned off while $i_{L1}$ reaches its maximum value $I_p$ (Fig. 3).

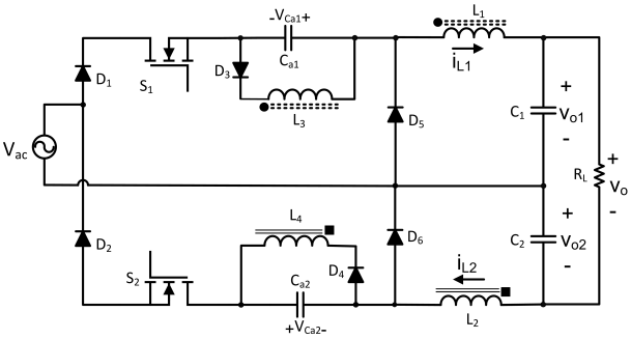



Fig. 1. Proposed bridgeless unity power factor buck rectifier.

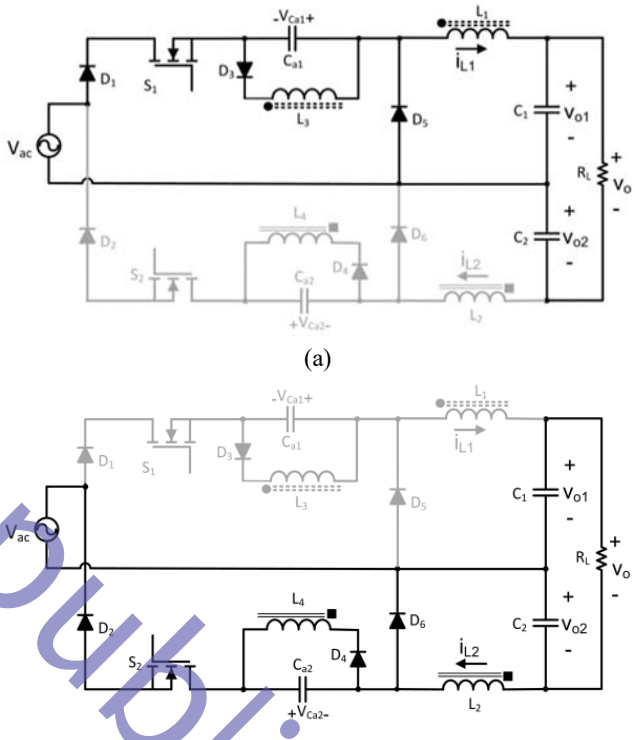



Fig. 2. Operation of the positive and negative half-line cycles. (a) Positive half-line cycle. (b) Negative half-line cycle.

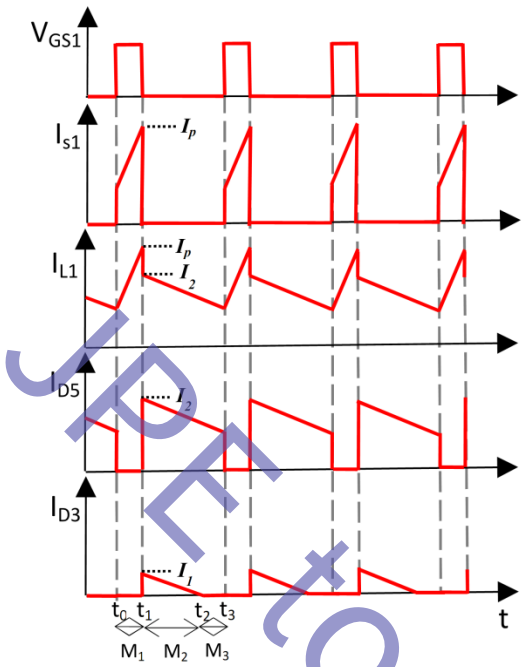



Fig. 3. Theoretical key waveforms.

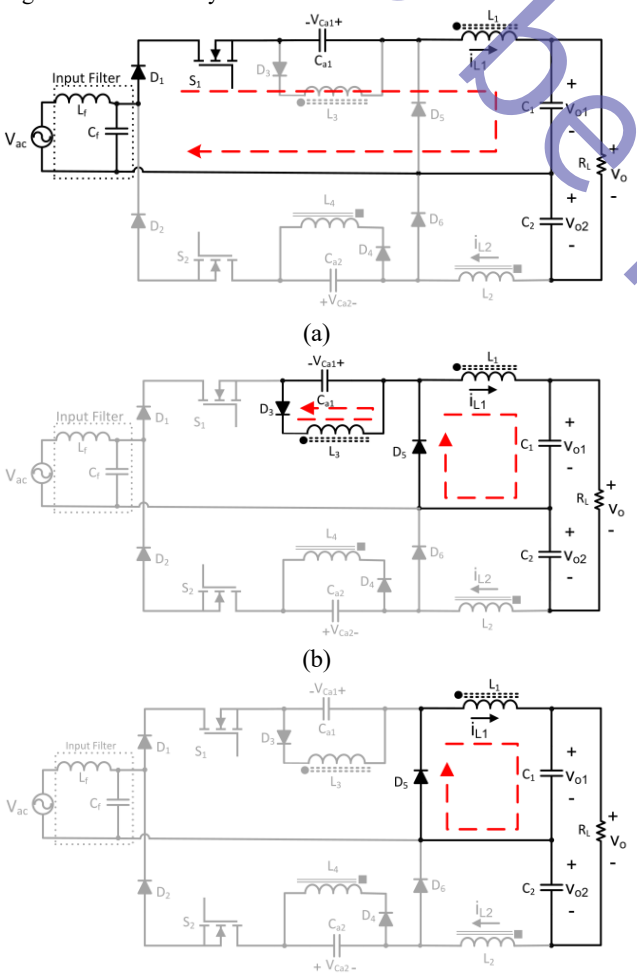



Fig. 4. Equivalent circuits of the three modes during the positive half-line cycle. (a) Mode 1. (b) Mode 2. (c) Mode 3.

*Mode 2* ($t_1$-$t_2$): Since $V_{Ca1}$ and $V_{O1}$ are almost equal, by turning the switch $S_1$ off, the diodes $D_3$ and $D_5$ conduct simultaneously (Fig. 4b). Thus, by turning the switch $S_1$ off, a part of the inductor $L_1$ energy charges the capacitor $C_{a1}$ and the other part charges the output capacitor $C_1$.

*Mode 3* ($t_2$-$t_3$): This mode starts when the capacitor $C_{a1}$ is charged up to $V_{O1}$ and the inductor current $i_{L3}$ is zero (Fig. 4c). The inductor current $i_{L1}$ freewheels through $D_5$ and supplies the load power. According to the operating modes, the buck converter shapes the line current for $V_{ac} < V_{O1}$ and the dead angle of the line current is omitted, which results a unity power factor.

In [3], [4] to provide low THD and high PF, a complex control circuit is applied. In the proposed rectifier, by eliminating the zero crossing dead angle, the conventional peak current control method can be applied. In this method, when the switch current reaches the reference current, the buck switch is turned off. After a switching period, it is turned on again to shape the input current.

In Table I, the proposed rectifier is compared with the topologies in [21]-[25]. According to Table I, just two simultaneously conducting semiconductor devices reduce the conduction losses and increase the efficiency.

TABLE I
COMPARISON OF THE PROPOSED RECTIFIER AND THE TOPOLOGIES IN [21]-[25]

| Parameters | [21] | [22] | [23],[24] | [25] | Proposed |
|---|---|---|---|---|---|
| **switch** | 2 | 2 | 2 | 1 | 2 |
| **diode** | 7 | 7 | 6 | 6 | 6 |
| **magnetic element** | 2 | 1 | 1 | 1 | 2 |
| **conducting semiconductor devices** | 4 | 3 | 4 | 3 | 2 |
| **Transition from flyback to buck at $V_{in} = V_{out}$** | yes | yes | yes | no | no |
| **bridgeless** | no | no | no | no | yes |

In the proposed converter, each buck inductor is coupled with its flyback counterpart. Therefore, the series capacitor voltages are equal to their corresponding output voltages, $V_{Ca1}=V_{O1}$ and $V_{Ca2}=V_{O2}$. As a result, in the both positive and negative half-line cycles, independent of the values of $V_{O1, 2}$ and $L_{1, 2}$, the line voltage $V_{ac}$ is applied to $L_{1, 2}$ and the dead angle of the buck converter is omitted. In addition, in order to achieve similar input current amplitudes for the positive and negative half cycles, due to the applied peak current control method, the values of $L_1$ and $L_2$ should be almost equal. Furthermore, $C_1$ and $C_2$ should be large enough to provide a small ripple and the difference in their values has minor effect in the converter operation.

## III. Design Procedure

According to the principle of operation, a simple design procedure is presented that includes the determination of the inductors, capacitors as well as the current and voltage stress of the semiconductor components.

### A. Minimum Duty Cycle

As expressed in mode 1, the capacitor $C_{a1}$ should be selected large enough to provide a low voltage ripple for $V_{Ca1}$. Thus, the inductor $L_1$ can be charged by the line voltage $V_{ac}$ in the time period of $DT$. By turning the buck switch $S_1$ off, a part of the inductor $L_1$ energy charges the capacitor $C_{a1}$ to the output voltage $V_{O1}$ in a short time. Then, the inductor $L_1$ is discharged by the output voltage $V_{O1}$ in the time period of $(1 - D)T$. Writing the volt-second balance for $L_1$ in the CCM as $V_{ac}D = V_{O1}(1 - D)$, the minimum duty cycle $D_{min}$ is expressed as (1). This shows that as line voltage increases, the duty cycle decreases and $D_{min}$ occurs for $V_{ac,max}$.

$$D_{\min} = \frac{V_{o1}}{V_{o1} + V_{ac,\max}} \tag{1}$$

### B. Auxiliary Capacitors $C_{a1,2}$

An input low pass filter should be designed to remove the switching component of the currents $i_{S1,2}$ and produce sinusoidal line current. Thus, its low cut-off frequency has been considered to be about 10% of the switching frequency and the inductor $L_f$ and the capacitor $C_f$ are selected. The average current of the buck switch in each switching cycle is equal to the instantaneous input current. Thus, the peak of the switch current $I_{in,peak}$ occurs at the peak of the line voltage.

$$I_{in,peak} = \frac{\sqrt{2}P_o}{V_{in,rms}} \tag{2}$$

Based on the above equation, the maximum area under the curve of the switch current ($S_i$) is obtained as (3), where $f_s$ is the switching frequency.

$$S_i = \frac{\sqrt{2}P_o}{f_s \times V_{in,rms}} \tag{3}$$

At the switch on time, $C_{a1}$ voltage is discharged from $V_{O1}$ to $V_{O1} - \Delta V_{Ca1}$. The maximum variation of $V_{Ca1}$ occurs at the maximum of the line voltage. Therefore, the capacitor $C_{a1}$ is calculated as (4).

$$C_{a1} = \frac{1}{\Delta V_{Ca1}} \times S_i = \frac{\sqrt{2}P_o}{f_s \times V_{in,rms} \times \Delta V_{Ca1}} \tag{4}$$

### C. Current and Voltage Stress of the Semiconductor Components

At the peak of the line voltage, the buck switch current $i_{S1}$ is increased with a slope of $V_{in,max}/L_1$ at the time period of $D_{min}T$ from $I_p$-$\Delta I_{L,max}$ to $I_p$, where $\Delta I_{L,max}$ is the maximum current ripple of the buck inductors (Fig. 3). The area under the curve of $i_{S1}$ on $D_{min}T$ is equal to $S_i$ and is presented in (3). In other words, the area of a trapezoidal current with a height of $D_{min}T$ and two bases of $I_p$ and $I_p - \Delta I_{L,max}$ is calculated as (5).

$$S_i = \frac{\left(I_P - \Delta I_{L,\max} + I_P\right) \times D_{\min}T}{2} \tag{5}$$

Using (3) and (5), the peak of the switch current $I_p$ is obtained from (6).

$$I_p = \frac{\sqrt{2}P_o}{V_{in,rms}D_{\min}} + \frac{1}{2}\Delta I_{L,\max} \tag{6}$$

In mode 1 (Fig. 4a), the freewheeling diode $D_5$ and the auxiliary flyback diode $D_3$ are off. Considering $V_{Ca1} = V_{O1}$, their reverse voltages are $V_{ac} + V_{O1}$. In mode 2 (Fig. 4b), by conducting the freewheeling diode $D_5$, the voltage stress of the buck switch $S_1$ is equal to $V_{ac} + V_{O1}$. It is observed that the voltage stress of the semiconductor components of the proposed converter can be as much as $V_{Ca1} = V_{O1} = V_O/2$ greater than the conventional buck converter.

### D. Detailed Analysis of the Second Operating Mode

As expressed in the second mode, the capacitor $C_{a1}$ should be large enough to provide a low voltage ripple for $V_{Ca1}$. Thus, the diodes $D_3$ and $D_5$ can be turned on simultaneously (Fig. 4b). Fig. 5 shows an equivalent circuit of this mode, where the magnetizing inductance and the leakage inductance of $L_{1,3}$ are shown by $L_M$ and $L_{lk}$, respectively. For the maximum of the line voltage $V_{ac,max}$, the initial voltage of $C_{a1}$ is $V_{O1}$ -$\Delta V_{Ca1}$ and the initial current of $L_M$ and $L_{lk}$ is equal to $I_p$.

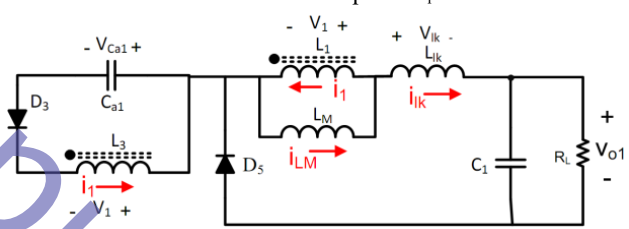



Fig. 5. An equivalent circuit of the second mode.

When the switch $S_1$ turns off, the voltage $V_1$ with the polarity shown in Fig. 5 is increased rapidly and clamped to $V_{O1}$- $\Delta V_{Ca1}$ + $V_{\gamma,D3}$ and the diode $D_3$ starts conducting. The leakage inductance $L_{lk}$ should continue its current. Thus, its voltage $V_{lk}$ is reversed and reaches $\Delta V_{Ca1}$, and the diode $D_5$ continues its current $i_{lk}$. The reverse voltage of $L_{lk}$ reduces the current $i_{lk}$ and considering a large $L_M$ and thus a constant $I_{LM}$, the current $i_1$ is increased. $\Delta V_{Ca1}$ should be small enough so that at the instant of current division between $i_1$ and $i_{lk}$, the current $i_{lk}$ does not reach zero and the current $i_1$ can charge the capacitor $C_{a1}$ to the voltage $V_{O1}$. To satisfy the above condition, the minimum value of the capacitor $C_{a1}$ should be calculated correctly. For this purpose, the voltages of the buck circuit are written as (7). The threshold voltage of the diodes $D_3$ and $D_5$ are assumed to be equal to ($V_\gamma$).

$$V_\gamma - V_1 + V_{lk} + V_{o1} = 0 \tag{7}$$

Writing $V_1$ as $V_{Ca1} + V_\gamma$ in the auxiliary flyback circuit, (7) can be rewritten as (8).

$$\Delta V_{Ca1} - \frac{1}{C_{a1}}\int i_1 dt - L_{lk}\frac{di_1}{dt} = 0 \tag{8}$$

By solving (8), the currents $i_1$ and $i_{lk}$ at the instant of current division are obtained as (9) and (10), respectively.

$$i_1(t) = k\sin(at) = \Delta V_{Ca1}\sqrt{\frac{C_{a1}}{L_{lk}}}\sin\left(\frac{1}{\sqrt{C_{a1}L_{lk}}}t\right) \quad (9)$$

$$i_{lk}(t) = I_{LM} - i_1(t) = I_{LM} - \Delta V_{Ca1}\sqrt{\frac{C_{a1}}{L_{lk}}}\sin\left(\frac{1}{\sqrt{C_{a1}L_{lk}}}t\right) \quad (10)$$

The current $i_{lk}$ should not reach zero ($i_{lk} > 0$) at the instant of current division of $I_{LM}$ between $i_{lk}$ and $i_1$ to satisfy the condition of the second mode operation. Therefore, the condition is written as (11).

$$\Delta V_{Ca1}\sqrt{\frac{C_{a1}}{L_{lk}}} < I_{LM} \quad (11)$$

Substituting $\Delta V_{Ca1}$ from (4) and $I_{LM}=I_p$ from (6) in (11), the minimum capacitance of $C_{a1}$ is obtained as (12).

$$C_{a1} \geq \frac{1}{L_k}\left(\frac{2\sqrt{2}P_o D_{\min} T}{2\sqrt{2}P_o + \Delta I_L V_{in,rms} D_{\min}}\right)^2 \quad (12)$$

Using the charging current of $C_{a1}$ presented in (9), the charging time $t'$ of $C_{a1}$ from $V_{o1}$-$\Delta V_{Ca1}$ to $V_{o1}$ is calculated from (13) and is shown in (14).

$$\Delta V_{Ca1} = \frac{1}{C_{a1}}\int_0^{t'} \Delta V_{Ca1}\sqrt{\frac{C_{a1}}{L_{lk}}}\sin\left(\frac{1}{\sqrt{C_{a1}L_{lk}}}t\right)dt \quad (13)$$

$$t' = \frac{\pi\sqrt{L_{lk}C_{a1}}}{2} \quad (14)$$

Thus, the amount of $i_1(t')$ and $i_{lk}(t')$ are calculated as (15) and (16).

$$I_1 = i_1(t') = \Delta V_{Ca1}\sqrt{\frac{C_{a1}}{L_{lk}}} \quad (15)$$

$$I_2 = i_{lk}(t') = I_p - \Delta V_{Ca1}\sqrt{\frac{C_{a1}}{L_{lk}}} \quad (16)$$

### *E. Buck Inductors*

Due to the eliminating of the zero crossing dead angle, buck inductor is charged by the line voltage. Thus, the buck inductor $L=L_1=L_2$ is calculated from (17).

$$L = \frac{\sqrt{2}V_{in,\text{rms}} \times D_{\min}}{\Delta I_{L,\max} \times f_s} \quad (17)$$

### *F. Output Capacitor*

The output capacitor of a PFC converter is calculated based on the output voltage ripple due to difference between instantaneous input and output voltage and is independent of the topology. Assuming unity power factor, the average input power is equal to $V_{\text{in,rms}} I_{\text{in,rms}}$, while instantaneous input power is equal to (18), where $f_l$ is the line frequency. The excess of input power, when the instantaneous input power is greater than the average input power, charges the output capacitor. Thus, the output capacitor based on the output voltage ripple is calculated as (19).

$$P_{in}(t) = 2V_{in,rms}I_{in,rms}\sin^2(2\pi f_l t) \quad (18)$$

$$C_o = \frac{P_o}{\Delta V_o \times V_o \times 2\pi f_l} \quad (19)$$

## IV. Experimental Results

In the buck PFC rectifiers presented in [2]-[4], due to zero crossing dead angle, there is a strong tradeoff between the PF and THD performance and output voltage level. Since the line current is zero for $V_{\text{in}} < V_{\text{out}}$, increasing the output voltage deteriorates the PF and THD. On the other hand, decreasing the output voltage increases the current levels of the rectifier and leads to higher conduction losses and lower efficiency. This tradeoff is resolved in the proposed converter by eliminating the zero crossing dead angle.

The performance of the proposed rectifier is verified using a 150 W, 48 V prototype circuit with a 110 $V_{ac}$ line voltage. The schematic of the implemented circuit is shown in Fig. 6.

For $V_O$=48 V, the average values of $V_{O1,2}$ are equal to 24 V (Fig. 6). Based on (1), the minimum duty cycle $D_{\min}$ at the peak of the line voltage $V_{ac,max}$=155 V is equal to 0.13. In the design of a regular buck converter, the current ripple of the buck inductor is considered about 20% of its maximum value. Due to the short ON time of the buck switches at the peak of the line voltage ($D_{\min}$=0.13) and restrictions on the response time of the

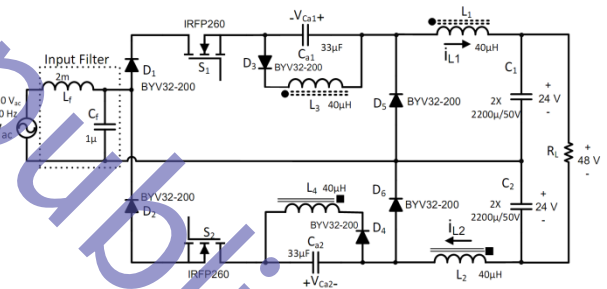



Fig. 6. Schematic of the implemented circuit.

elements of the control circuit, the maximum inductor current ripple $\Delta I_{\text{L,max}}$ is considered about 60% of the maximum inductor current $I_p$. As a result, the current control loop can follow the changes of the inductor current well. Thus, based on (6), for $P_o$=150 W, the maximum inductor current $I_p$ is equal to 21 A and $\Delta I_{\text{L,max}}$ is 12.5 A. Based on (17), for $f_s$=40 kHz, the buck inductors $L=L_1=L_2$ are equal to 40 µH. To implement the coupled inductors $L_{1,3}$ and $L_{2,4}$ with a unity turn ratio, two ferrite cores (EE33/29) with 50 turns of wire are used. The measured leakage inductance of the coupled inductors is about 0.5 µH.

Based on (12), the condition of the second mode of operation is that the auxiliary flyback capacitors $C_{a1,2}$ should be greater than 10 µF. To ensure the second mode operation, 33 µF electrolyte capacitors are used for $C_{a1,2}$ and $\Delta V_{Ca1,2}$=1.5 V is

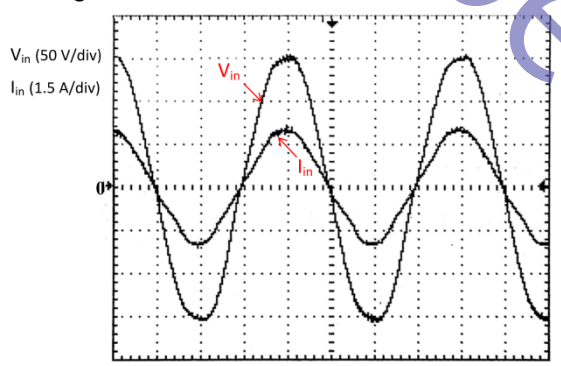
obtained from (4). According to (15) and (16), the currents $I_1$ and $I_2$ are equal to 10 and 11 A, respectively (Fig. 3).

The voltage stress of the switches and diodes was determined as $V_{ac}$+ $V_{O1}$=180 V. The peak current of $S_1$ and $D_1$ is $I_p$=21 A, while the auxiliary diode $D_3$ and the freewheeling diode $D_5$ are $I_1$=10 A and $I_2$=11 A, respectively. Therefore, IRFP260 MOSFET switches and BYV32-200 diodes were used for all of the semiconductor devices.

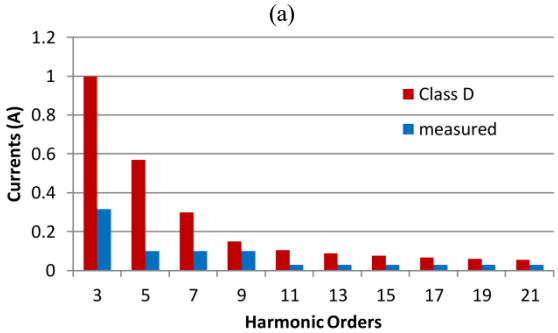
From (19), for $P_o$=150 W, $V_O$=48 V and $\Delta V_O$=5 V, the output capacitor $C_O$ is equal to 2 mF. Two electrolyte capacitors (2200 μF, 50 VDC) were used for the output capacitors $C_1$ and $C_2$.

The cut-off frequency of the input low pass filter ($L_f$ and $C_f$) has been set to about 10% of the switching frequency to remove the switching component of the currents $i_{S1,2}$, which results in a sinusoidal line current. Thus, $L_f$=2 mH and $C_f$=1 μF have been chosen.

Fig. 7a shows the measured line current and voltage waveforms at 150 W of output power. It is observed that the zero crossing dead angle of the line current has been omitted. As a result, a near unity power factor has been obtained. Compliance of the measured line current harmonics, at 150 W of output power and 110 $V_{ac}$ of line voltage, with the Class D requirements of JIS C 6100-3-2 (corresponding to the Japanese specifications of IEC 61000-3-2 for a 110 $V_{ac}$ line voltage) is given in Fig. 7b.



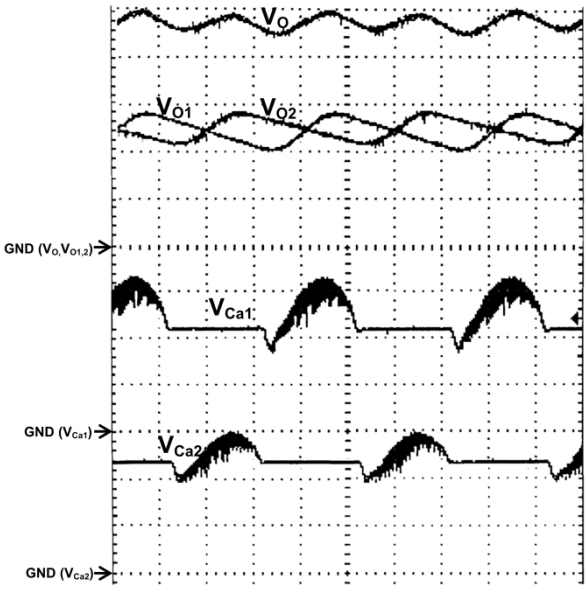

(a)




(b)

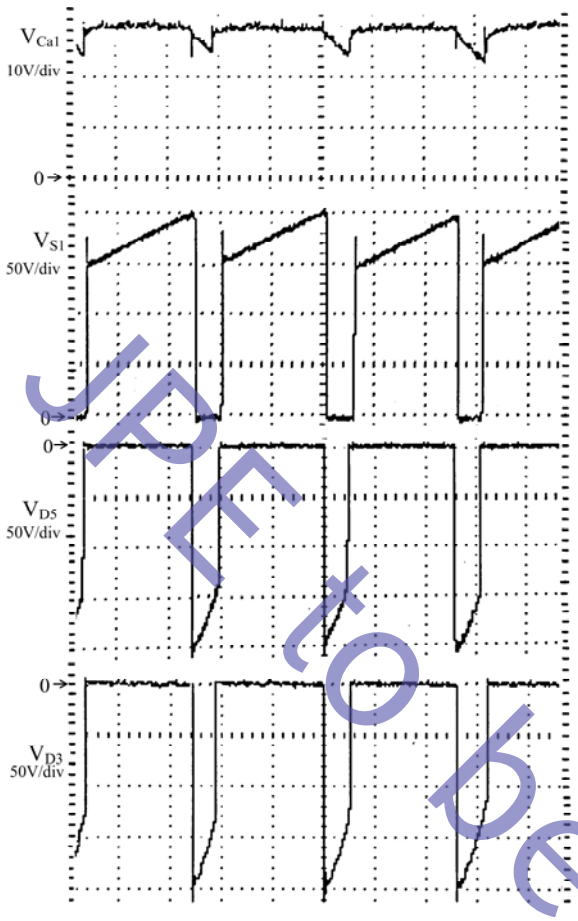
Fig. 7. Measured line waveforms at Po=150 W. (a) Line current and voltage waveforms (time: 5 ms/div). (b) Measured odd harmonic components of the line current with the Class D requirements of JIS C 6100-3-2.

Fig. 8a shows the measured low frequency voltages of $V_O$, $V_{O1,2}$ and $V_{Ca1,2}$. It can be observed that the output voltage of each auxiliary flyback converter $V_{Ca1,2}$ follows the corresponding output voltage $V_{O1,2}$ of the buck converter. Thus, the line voltage $V_{ac}$ is applied to each of the buck inductors and the dead angle of the line current is omitted.



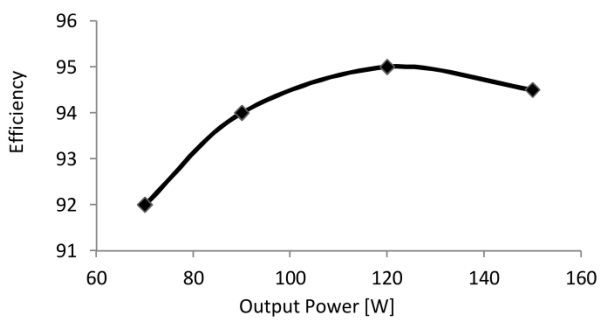

(a)


(b)

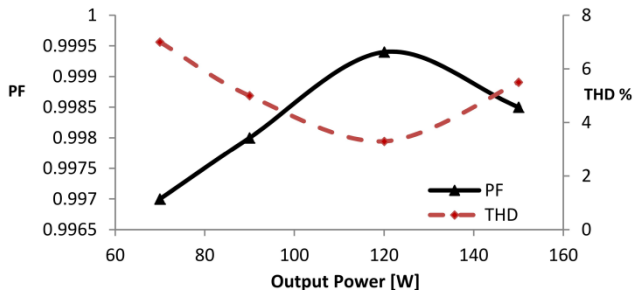



(c)

Fig. 8. Measured waveforms at Po=150 W. (a) Low frequency voltages (10 V/div; time: 5 ms/div). (b) Switching currents at the peak of the line voltage (8 A/div; time: 10 μs/div). (c) Switching voltages at the peak of the line voltage (time: 10 μs/div).




(a) Efficiency.




(b) PF and THD.

Fig. 9. Measured efficiency, PF and THD compared with output power.

Experimental results show that the peak of the positive and negative line currents in Fig. 7a and the voltages $V_{O1}$ and $V_{O2}$ in Fig. 8a are well balance with each other. Therefore, for the values of the inductors $L_1$ and $L_2$ with small mismatching, the effect of mismatching of the buck inductors is negligible.

Measured switching current and voltage waveforms at the peak of the line voltage for 150 W of output power are shown in Figs. 8b and 8c. The waveforms and the mount of currents and voltages are in agreement with the theoretical ones shown in Fig. 3 and the designed values.

The measured efficiency, PF and THD at different output powers are shown in Fig. 9. The small existing distortion at the line current zero crossing slightly increases the THD, especially for a small line current amplitude. Thus, the amount of THD of the line current is increased with a decreasing of the rectifier power as shown in Fig. 9b. In addition, at a high output power, a higher voltage ripple of $C_{a1}$ and $C_{a2}$ slightly increases the THD.

A comparison of the PF, THD and efficiency of the proposed rectifier and state-of-the-art buck PFC converters for a 110 Vac line voltage is presented in Table II. It can be seen that the proposed converter with a simple auxiliary flyback converter and without an auxiliary switch has a PF of more than 0.997 and a THD of less than 7%. By eliminating the input bridge diodes, the number of conducting semiconductor elements in the inductor charging path has been reduced from 3 or 4 to 2 when compared with the topologies in [21]-[25]. This feature decreases the conduction losses. Hence, it increases the efficiency so that the proposed converter shows a high efficiency of around 94%.

TABLE II

COMPARISON OF THE PF, THD AND EFFICIENCY OF THE PROPOSED RECTIFIER AND STATE-OF-THE-ART BUCK RECTIFIERS FOR 110 VAC LINE VOLTAGE

| Ref. | Spec. | PF | THD (%) | Efficiency (%) |
|---|---|---|---|---|
| [2] | $V_O$=90V, $P_O$=100W | 0.9 | - | 97 |
| [3] | $V_O$=80V, $P_O$=94W | 0.93 | - | 96 |

| | | | | |
|---|---|---|---|---|
| [4] | $V_O$=160V, $P_O$=75W | 0.92 | 31.3 | 97 |
| [23] | $V_O$=80V, $P_O$=150W | 0.99 | 7.6 | 95 |
| [24] | $V_O$=80V, $P_O$=100W | 0.99 | - | 93.6 |
| [25] | $V_O$=48V, $P_O$=30W | 0.99 | 5 | 92.5 |
| Proposed | $V_O$=48V, $P_O$=150W | 0.998 | 5 | 94.5 |

## V. CONCLUSIONS

This paper presented a bridgeless unity power factor buck rectifier. It is shown that without any special design requirements, the dead angle of the buck rectifier can be eliminated. As a result, a unity power factor and a high efficiency can be achieved. A detailed theoretical analysis and design procedure have been presented and verified by experimental results obtained on a 150 W, 48 V output prototype, and 110 V line voltage. Thus, the proposed converter can achieve a unity power factor, a THD of less than 7% and a high efficiency of around 94%.

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**Mahdi Malekanehrad** was born in Birjand, Iran, in 1987. He received his B.S. degree in Electrical Engineering from Hakim Sabzevari University, Sabzevar, Iran, in 2009; and his M.S. degree from the Isfahan University of Technology, Isfahan, Iran, in 2012, where he is presently working towards his Ph.D. degree in Electrical Engineering. His current research interests include power factor correction converters and soft-switching techniques in DC–DC converters.

**Ehsan Adib** was born in Isfahan, Iran, in 1982. He received his B.S., M.S. and Ph.D. degrees in Electrical Engineering from the Isfahan University of Technology, Isfahan, Iran, in 2003, 2006 and 2009, respectively. He is presently working as a faculty member in the Department of Electrical and Computer Engineering, Isfahan University of Technology. He is the author of more than 100 papers published in journals and conference proceedings. His current research interests include DC–DC converters and their applications, and soft-switching techniques.