

A Passive Lossless Soft-Switching Single Inductor Dual Buck Full-Bridge Inverter

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Abstract

A novel passive lossless soft-switching single inductor dual buck full-bridge inverter (PLSSIDBFBI) is presented in this paper. To accomplish this, a passive lossless snubber circuit is added to a dual buck full-bridge inverter. Therefore, the advantages of the dual buck full-bridge inverter are included in the proposed inverter, and the inverter has just one filter inductor, which can decrease the system volume and improve the integration. In addition, the passive lossless snubber circuit achieves soft-switching by its own resonance, and all of the energy stored in the passive lossless snubber circuit can be transferred to load. A comparison between eight topologies is performed in this paper, and the analysis shows that the proposed soft-switching inverter topology has high reliability and efficiency. Finally, experimental results obtained with a 1 kW prototype verify the theoretical analysis and demonstrate the prominent characteristics of a reduced switching loss and improved efficiency.

Key words: Dual buck, High efficiency, High reliability, Passive lossless, Single inductor, Soft-switching

I. INTRODUCTION

In recent years, transformerless photovoltaic (PV) grid-connected inverters have drawn a lot of attention for use in distributed PV power generation systems due to their low cost, compact structure, high reliability and high conversion efficiency [1]-[4]. The study of transformerless PV grid-connected inverters always focuses on optimizing the topology and improving reliability on the premise of guaranteeing the high-efficiency advantage of transformerless PV grid-connected inverters. With the continuous increase in the requirements for conversion efficiency, improving the switching frequency of power switching devices to downsize the filter and improve the power density has become the inevitable choice for transformerless PV grid-connected inverters. However, with the growing demands on the frequency of power electronic equipment, the switching losses of power devices have become an increasingly prominent problem. An efficient approach to solve the switching dissipation problem and to improve system efficiency is to use

soft-switching techniques [5], [6]. The concept of the soft switching technique for inverters was first proposed by Dr. Divan [7]. After years of development, they can be classified into resonant link dc-ac inverters, resonant transition dc-ac inverters, and load resonant dc-ac inverters^{[8]-[10]}. Based on the availability of auxiliary switching devices, soft-switching technology can be divided into two categories: active soft-switching and passive soft-switching. The authors of [11] used a coupled-magnetic structure as the auxiliary resonant snubber circuit to achieve zero-voltage switching (ZVS). The auxiliary devices are low current and low cost IGBTs and diodes, which have low conduction and switching losses. The authors of [12]-[14] proposed ZCT-H6-I, ZVT-H6-I and SLF-H6-I active soft-switching transformerless inverters, which were developed from the H6 topology. In these topologies, the switching losses in the switches and diodes have been decreased based on the perfect leakage current suppression performance. The ZVT-HERIC active soft-switching transformerless inverter was presented in [15], by integrating resonant tanks and freewheeling switches. The zero voltage transition (ZVT) for all of the high-frequency switches and auxiliary switches were achieved, which can also alleviate the reverse-recovery problem for all of the diodes and reduce the voltage stress. However, according to an analysis of reliability in [16], the active devices have negative effects on the reliability of the system. In addition, the active soft-switching techniques

implemented by adding auxiliary switches or changing the topology have problems in terms of difficult modulation, high voltage or current stress, large number of resonant components and large losses. Therefore, a snubber circuit is the only way to achieve soft switching without active devices. In snubber circuits, the power circuits of main switches are connected in parallel with the capacitive branch or in series with the inductor elements to avoid withstanding high voltage and high current. Thus, passive soft-switching technology based on the snubber circuit has attracted more attention due to its characteristics of no additional auxiliary switches or corresponding control circuits, less additional loss and high reliability. The authors of [17] proposed a soft-switching three-level inverter that reduced the switching losses with very few passive devices. In [18], lossless passive soft-switching properties and synthesis procedures that are appropriate for all PWM converters are introduced. In addition, the full-bridge and half-bridge soft-switching inverter topologies were also deduced to verify the correctness of principle along with its characteristics of the simple structure and low voltage stress.

Another way to increase system efficiency is by using a simple and efficient topology. The dual buck inverter [19] exploited in recent years is different from full-bridge or half-bridge inverters, and the topology is shown in Fig. 1. The inverter has no shoot-through problem or reverse recovery problem of the body diode, which reduces the reverse recovery loss and increases the system efficiency. In order to improve voltage utilization and reduce the voltage stress based on dual buck inverters, the multi-level dual buck inverters including the diode clamped type and flying capacitor type were studied in [19]-[21], and the dual buck full-bridge-type inverters were proposed in [22]-[23]. However, conventional dual buck inverters [19]-[23] still have an inherent weakness in terms of requiring two or more inductors, which increases the volume and cost of the system. On the basis of the dual buck topology, a single-inductor dual buck full-bridge inverter was proposed, which preserved the advantages of dual buck inverters [18]-[23]. The voltage reversal bridge structure is used to make the DC input side remove a large voltage divider to increase the DC voltage utilization. In addition, the inverter only uses a single inductor for filtering, which reduces the volume and weight of the system and improves the integration.

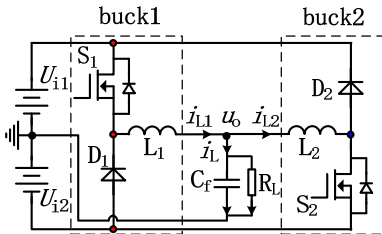


Fig. 1. Dual buck half-bridge inverter.

According to the above-mentioned ideas, this paper proposes a new topology called the passive lossless soft-

switching single inductor dual buck full-bridge inverter (PLSSIDBFBI). This topology retains the advantages of no shoot-through problem, no body diode reverse recovery problem, high input voltage utilization rate and using one filter inductor. The high-frequency main switches realize lossless soft switching by adding snubber circuits, and the snubber circuits have no resistors or switches, which makes the topology simple and system reliability high.

II. OPERATING PRINCIPLE

The topology of the PLSSIDBFBI is shown in Fig. Fig. 2. The PLSSIDBFBI has two stages, the preceding stage introduces a full-bridge circuit to achieve commutation of the input voltage, and the second stage performs high-frequency chopping modulation through switches S_a and S_b . In addition, one inductor, two capacitors and three diodes compose a passive lossless snubber circuit. The proposed topology works in the half-cycle mode with a parallel structure constituted by two Buck circuits, where Buck I consists of S_2 , S_3 , S_a , D_1 , L and C_f , and Buck II consists of S_1 , S_4 , S_b , D_2 , L and C_f . The two Buck circuits operate alternately in one power-frequency cycle, where D_1 and D_2 provide the freewheeling circuit for the inductor current when $i_L > 0$ and $i_L < 0$.

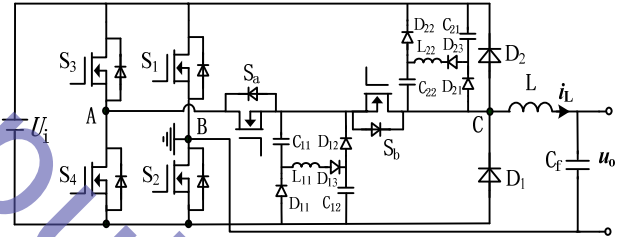


Fig. 2. Passive lossless soft-switching single inductor dual buck full-bridge inverter.

Since the switching frequency, voltage and current applied on switches S_a and S_b are high, the two switches produce considerable switching loss. Therefore, adding passive devices on the power circuits is a dominant solution to decrease the peak voltage and current of the switches and to reduce the switching loss.

Operating waveforms of the PLSSIDBFBI and snubber circuit are shown in Fig. 3 and Fig. 4. The corresponding operating modes are shown in Fig. 5.

A. t_0-t_1

During this stage, $i_L > 0$, $u_o > 0$. Buck I circuit works in the PWM mode while Buck II is suspended. Two modes are included in the operating process:

1) *Working Mode 1*: As shown in Fig. 5(a), S_1 and S_4 are turned off, while S_2 , S_3 , S_a and S_b are turned on. The output current i_L rises linearly.

During this mode, the voltage and current waveforms of S_a (i_{s_a} , u_{s_a}) are shown in Fig. 4, in the duration from t_0 to t_2 . As the figure shows, u_{s_a} declines rapidly to zero. i_{s_a} keeps rising

to charge both the load and the series branch (C_{12} - L_{11} - D_{13} - C_{11}) in the snubber circuit. The L_{11} performances resonant behavior with C_{11} and C_{12} , and the resonance frequency can be expressed as:

$$\omega = \frac{1}{\sqrt{L_{11}[C_{11}C_{12}/(C_{11} + C_{12})]}} \quad (1)$$

The currents i_{sa} and i_{L11} (current through L_{11}) change in accordance with a second order oscillation. In addition, after half of a resonant cycle, i_{L11} decreases from positive to negative through the zero-crossing point, and D_{13} becomes reverse-biased at t_0 , which is the end of the resonant operation. The current through L_{11} during the resonance can be obtained from:

$$i_{L11}(t) = \frac{U_i}{Z_0} \sin \omega(t - t_0) \quad (2)$$

where, Z_0 is the equivalent impedance of L_{11} , C_{11} and C_{12} ; U_i is the input voltage; and there is:

$$Z_0 = \sqrt{L_{11}[C_{11}C_{12}/(C_{11} + C_{12})]} \quad (3)$$

The sum of the voltages across C_{11} and C_{12} can be expressed as:

$$u_c(t) = U_i - U_i \cos \omega(t - t_0) \quad (4)$$

$$u_{C11}(t) = \frac{C_{12}}{C_{11} + C_{12}} u_c(t) \quad (5)$$

$$u_{C12}(t) = \frac{C_{11}}{C_{11} + C_{12}} u_c(t) \quad (6)$$

When $C_{11}=C_{12}$, the voltages across C_{11} and C_{12} are both U_i at t_1 .

2) *Working Mode 2*: As shown in Fig. 5(b), S_a is turned off, S_1 and S_4 remain in the turn-off state, while S_2 , S_3 and S_b remain in the turn-on state. D_1 is the freewheeling diode that is forward biased to maintain the output current. The output current i_L decreases linearly.

During this mode, the voltage and current waveforms of S_a (i_{sa} , u_{sa}) are shown in Fig. 4, in the duration from t_2 to t_4 . At $t=t_2$, i_{sa} decreases. The two parallel branches composed of (C_{11} , D_{11}) and (C_{12} , D_{12}) can be regarded as a parallel connection with the switch S_1 through the input voltage U_i . Since the voltages across the capacitors C_{11} and C_{12} cannot appear to mutate, the Zero-Voltage-Switching (ZVS) turn-off of S_a can be achieved.

When S_a is turned off softly, C_{11} and C_{12} begin to discharge. u_{sa} rises from zero, and the voltage across S_a can be expressed as:

$$u_{sa}(t) = U_i - U_{C11}(t) \quad (7)$$

The discharge process continues until t_3 , when u_{C11} and u_{C12} decline to zero and u_{s1} rises to U_i .

B. t_1 - t_2

During this stage, $i_L < 0$, $u_o < 0$. Buck II works in the PWM mode while Buck I is suspended. Two modes are included in the operating process:

3) *Working Mode 3*: As shown in Fig. 5(c), S_1 , S_4 , S_a and S_b are turned on, while S_2 is turned off. The output current i_L rises linearly.

During this mode, the voltage and current waveforms of S_b (i_{sb} , u_{sb}) are similar to those of S_a , as shown in Fig. 4, from t_0 to t_2 . i_{sb} charges both the load and the series branch (C_{21} - D_{23} - L_{22} - C_{22}) in the snubber circuit.

4) *Working Mode 4*: As shown in Fig. 5(d), S_b is turned off, and S_2 and S_3 remain in the turn-off state, while S_1 , S_4 and S_a remain in the turn-on state. D_2 is the freewheeling diode that is forward-biased to maintain the output current. The output current i_L decreases linearly.

During this mode, the voltage and current waveforms of S_b (i_{sb} , u_{sb}) are similar to those of S_a , as shown in Fig. 4, from t_2 to t_4 . The two parallel branches composed of (C_{21} , D_{21}) and (C_{22} , D_{22}) can be regarded as being in parallel connection with the switch S_b through the input voltage U_i . The energy stored in the capacitors C_{21} and C_{22} is transferred to the load. In addition, the Zero-Voltage-Switching (ZVS) turn-off of S_b can be achieved.

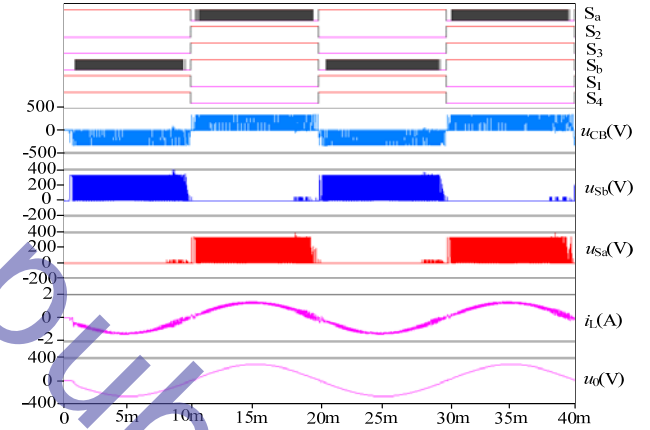


Fig. 3. Key waveforms of the passive lossless soft-switching dual buck full-bridge inverter.

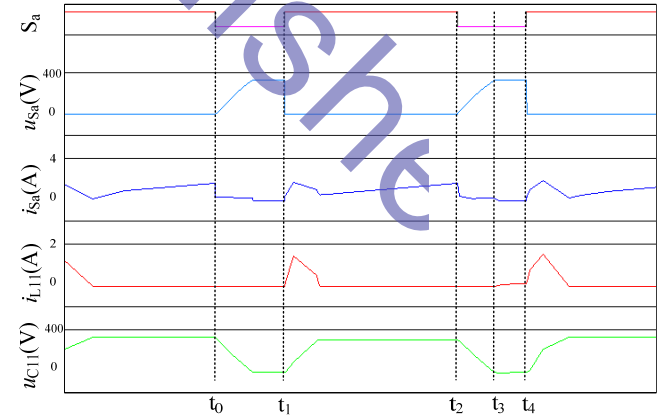


Fig. 4. Key waveforms of a snubber circuit.

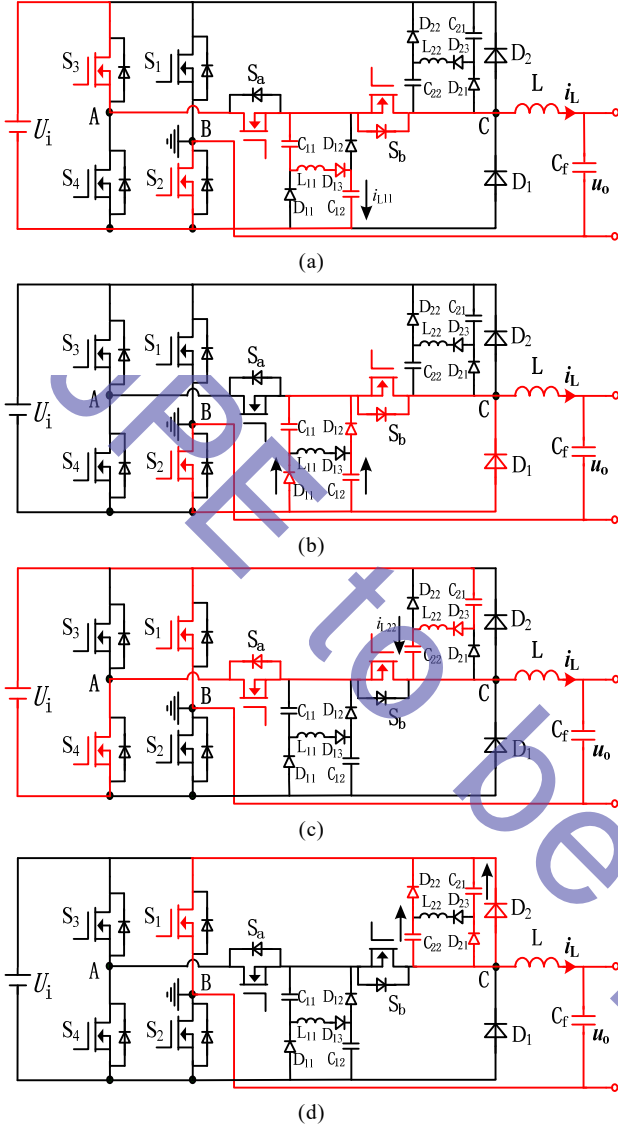


Fig. 5. Operating modes of the passive lossless soft-switching dual buck full bridge inverter. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4.

III. PARAMETER DESIGN OF THE SNUBBER CIRCUIT AND LOSS ANALYSIS

A. Parameter Design of the Snubber Circuit

In case of the specified parameters of the main circuit, the capacitances and inductances in the snubber circuit have a great effect on the operation performance of the topology. Taking S_a as an example, simulation waveforms of the snubber circuit with different capacitances and inductances are shown in Fig. 6 and Fig. 7.

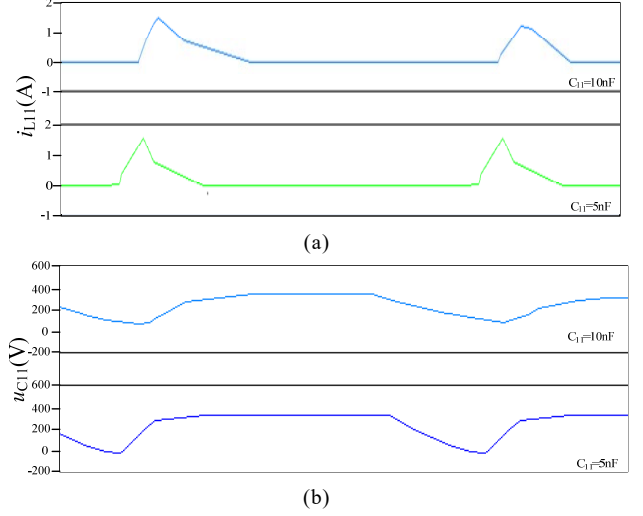


Fig. 6. Simulation waveforms of the snubber circuit with different capacitances. (a) Oscillating current i_{L11} . (b) Capacitor voltage u_{C11} .

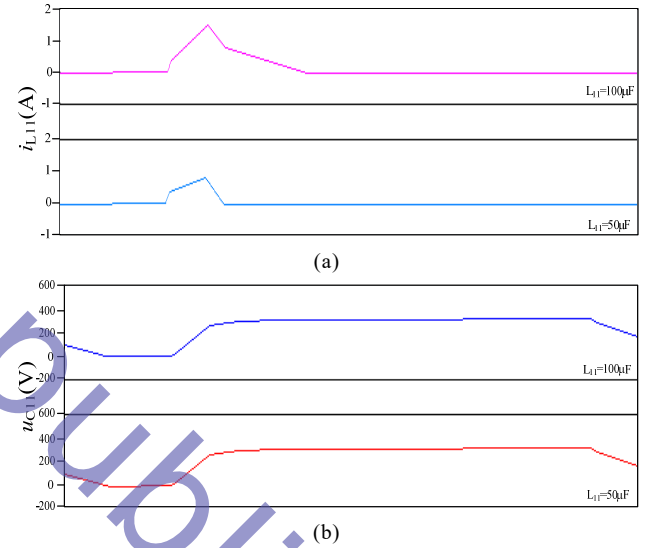


Fig. 7. Simulation waveforms of the snubber circuit with different inductances. (a) Oscillating current i_{L11} . (b) Capacitor voltage u_{C11} .

As shown in Fig. 6(b), the discharging rate of C_{11} decreases with an increase of C_{11} . In other words, the decreasing rate of u_{C11} and the increasing rate of u_{S_a} both slow down. Therefore, the switch loss of S_a is reduced. However, an increase of C_{11} increases the current through S_a and oscillating period, which can be seen from Fig. 6(a).

As shown in Fig. 7, the current through S_a decreases with an increase of L_{11} . However, the oscillating period increases.

Consequently, the values of C_{11} , C_{12} and L_{11} are direct influence factors for the operation of circuit. In addition, the values are restricted by the current withstand capability and switch-on time of the power switch.

The peak oscillating current of the snubber circuit during the conduction period of S_a can be expressed as:

$$i_{L11\max} = \frac{U_i}{Z_0} = U_i \sqrt{C_{11}/2L_{11}} \quad (8)$$

When S_a is turned on, the current through S_a can be expressed as:

$$i_{S_a} = i_{L_{11}} + i_L \quad (9)$$

where, i_L is the current through the inductor L , and $i_{L_{11}}$ is the oscillating current through the inductor L_{11} .

Since the peak oscillating current has the feature of $I_{S_{a\max}} > I_{L_{11\max}}$, the value of L_{11} can be expressed as:

$$L_{11} > \frac{U_i C_{11}}{2i_{S_{a\max}}^2} \quad (10)$$

The values of C_{11} , C_{12} and L_{11} are also restricted by the switch-on time of the power switch. In order to ensure that C_{11} and C_{12} are charged to U_i , the half resonant process should be finished in the switch-on time of S_a , that is:

$$\frac{\pi}{\omega} \leq T_{on\min} \quad (11)$$

where, ω is the resonant angular frequency, and $T_{on\min}$ is minimum switch-on time of the power switch.

When $C_{11} = C_{12}$:

$$T_{on\min} \geq \pi \sqrt{L_{11} (C_{11}/2)} \quad (12)$$

When the duty ratio of S_a is tiny, the half resonant process cannot be realized. However, the inductor current and the turn-off loss of the power switch are small at this moment. Setting the switching frequency to $f_s = 60$ kHz and $T_{on\min} = 0.6 \mu s$ in the experiment, there is $T_s = 6 \mu s$.

With the introduction of a snubber circuit, the turn-off loss of the power switch is reduced. However, the conduction loss increases for the oscillating current. Therefore, the influence of the system loss should be taken into consideration to design the parameters of C_{11} , C_{12} and L_{11} .

In one switching cycle, the turn-off loss of the power switch S_a can be obtained from:

$$P_{S_{off}} = \frac{1}{T} \sum_{i=1}^{N_s} \left[\frac{1}{2} U_i(i) i_{S_a}(i) \frac{t_{fr}^2(i)}{t_{fr}(i) + t_f(i)} + \frac{5}{6} U_{FR}(i) i_{S_a}(i) \frac{t_{fr}^2(i)}{t_{fr}(i) + t_f(i)} \right] \quad (13)$$

where, N_s is the switching time of the power switches per cycle, $i_{S_a}(i)$ is the current through S_a before the i^{th} turn-off of S_a , $U_i(i)$ is the voltage across S_a before the i^{th} turn-off of S_a , $t_f(i)$ is the fall time of S_a before the i^{th} turn-off of S_a , and $t_{fr}(i)$ and $U_{FR}(i)$ are the rise time and forward peak voltage of the diode when it becomes forward-biased for the i^{th} time.

The conduction loss of the power switch S_a can be expressed as:

$$P_{S_{on-state}} = \frac{1}{T} \sum_{i=0}^{N_s} \int_0^{D(i)T_s(i)} i_{on-state}^2(i) R_{ds(on)} dt \quad (14)$$

where, $T_s(i)$ is the switching period, $D(i)$ is the duty ratio, $i_{on-state}(i)$ is the current through S_a when S_a is turned on for the i^{th} time, and $R_{ds(on)}(i)$ is the on-resistance of S_a .

According to the parameters of the power switch and diode, the increment in the conduction loss of the power switch S_a

after adding the snubber circuit can be calculated as:

$$\Delta P_{S_{on-state}} = \frac{1}{T} \sum_{i=0}^{N_s} \int_0^{D(i)T_s(i)} [i_{L_{11}}^2(i) + 2i_{L_{11}}(i)i_L(i)] R_{ds(on)} dt \quad (15)$$

The increment in the turn-off loss of the power switch S_a can be obtained as:

$$\Delta P_{S_{off}} = \frac{1}{T} \sum_{i=1}^{N_s} \left[-\frac{1}{4} U_i i_{L_{11}}(i) \frac{t_{fr}^2(i)}{t_{fr}(i) + t_f(i)} \right] \quad (16)$$

To make the added snubber circuit helpful for decreasing the system loss, the increment of the conduction loss must be less than the increment of the turn-off loss. Accordingly, there is:

$$\int_0^{D(i)T_s(i)} \left[\frac{i_{L_{11}}^2(i)}{i_L(i)} + 2i_{L_{11}}(i) \right] R_{ds(on)} dt < \frac{1}{4} U_i \frac{t_{fr}^2(i)}{t_{fr}(i) + t_f(i)} \quad (17)$$

From (8) and (17), equation (18) can be derived as:

$$\frac{U_i C_{11}}{2L_{11}} + \sqrt{2C_{11}/L_{11}} < \frac{1}{2T_s R_{ds(on)}} \frac{t_{fr}^2(i)}{t_{fr}(i) + t_f(i)} \quad (18)$$

B. Loss Analysis

In general, the total losses of transformerless inverters are composed of the switching and conduction loss of the power switches and power diodes along with the hysteresis loss (P_{Fe}) and copper loss (P_{Cu}) of the inductors. In the proposed PLSSIDBFBI, the total losses mainly consist of the followings: the four switches in the full-bridge circuit switch only once per power-frequency cycle, the switching loss can be ignored and only the conduction loss needs to be considered. According to the parameter design of the snubber circuit in chapter III, the two high-frequency switches cannot be turned off softly when $D_{TO} < 0.1$. However, only the turn-on loss and conduction loss need to be considered since both the inductor current and the switching loss of the switches are small. To power the diodes, only the turn-off loss and conduction loss need to be considered because in one buck circuit, the turn-on of the high-frequency switches means the turn-off of the corresponding power diodes. Conversely, the turn-off of the power diodes means the turn-off of the high-frequency switches. According to the theoretical loss analysis of inverters in [28], the conduction loss of the switches is shown in equation (14), and the turn-on loss can be expressed as:

$$P_{S_{on}} = \frac{1}{T} \sum_{i=0}^{N_s} \left[\frac{1}{2} U_i i_{S_a}(i) t_r(i) + \frac{2}{3} U_i I_{RM}(i) t_{rr}(i) \right] \quad (19)$$

Further, the turn-off loss of the corresponding diodes can be obtained as:

$$P_{D_{off}} = \frac{1}{T} \sum_{i=0}^{N_s} \left\{ \begin{aligned} &U_F(i) [i_{S_a}(i) + I_{RM}(i)] t_r(i) \\ &+ \frac{1}{4} U_F(i) i_{S_a}(i) t_{rr}(i) + \frac{1}{3} U_i I_{RM}(i) t_{rr}(i) \end{aligned} \right\} \quad (20)$$

where, $I_{RM}(i)$ is the peak reverse recovery current of the diode, $t_r(i)$ is the rise time of the switch turned on for the i^{th} time, and $t_{rr}(i)$ is the reverse recovery time of the diode turned off for the i^{th} time.

The conduction loss of the diodes can be expressed as:

$$P_{Dcon} = \frac{1}{T} \sum_{i=0}^{N_s} \int_0^{(1-D(i))T_s(i)} i_{Don}(i) U_F(i) dt \quad (21)$$

where, $i_{Don}(i)$ is the current through the diode during the i^{th} switching process, and $U_F(i)$ is the forward voltage drop of the diode.

The hysteresis loss of the inductor can be obtained from the improved Steinmetts equation:

$$P_{Fe} = f(C_m f_{eq}^{\alpha-1} \Delta B^\beta) \quad (22)$$

where f is the switching frequency, ΔB is the amplitude of the magnetic flux density, and α and β are experienced parameters provided by the data sheets of the magnetic core. In addition, there is:

$$f_{eq} = \frac{2f}{D(1-D)\pi^2} \quad (23)$$

The copper loss of the inductor is determined by the equivalent resistance R_L of the inductor as:

$$p_{cu} = I_L^2 R_L = I_L^2 \rho_{cu} \frac{Len}{Csa} \quad (24)$$

where, ρ_{cu} is the resistivity of the copper wires, Len is the length of the copper wires, and Csa is the sectional area of the copper wires.

By plugging the prototype parameters of the proposed buck inverter into the above equations, a pie chart of the losses compositions at a full load can be drawn as shown in Fig. 8.

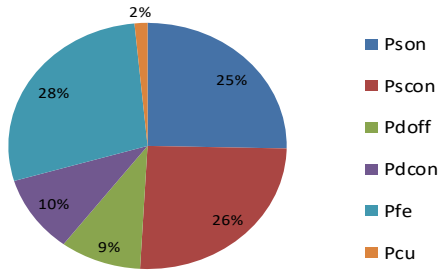


Fig. 8. Losses compositions at a full load.

IV. RELIABILITY ANALYSIS

In addition to efficiency, reliability is another important factor for evaluating a topology. The number of devices has the major influence on system reliability. When this number is reduced, the topology and control method are simplified, and the failure rate becomes smaller. Generally, when compared with active devices, passive devices have a higher reliability.

In order to quantitatively calculate the reliability of the

topology, the MIL-HDBK-217 handbook is used for reliability prediction. Based on reliability engineering theory, the reliability R_P of a system can be calculated as:

$$R_P = \prod_{i=1}^n R_i \quad (25)$$

$$R_i = \exp(-\lambda_{pi} t) \quad (26)$$

where, R_i is the individual reliability of the involved components, and λ_{pi} is the actual failure rate of the device, which is given by:

$$\lambda_p = \lambda_b \prod_{i=1}^m \pi_i \quad (27)$$

where, π_i is the modifying factors of each device, m is the number of modifying factors, and λ_b is the basic failure rate of the electronic devices.

TABLE I
MODIFYING FACTORS

Factors	Switch	Diode	Capacitor	Inductor
π_T	○	○	○	
π_Q	○	○	○	○
π_E	○	○	○	○
π_A	○			
π_L				○
π_C			○	
π_V			○	
π_S		○		

Usually, power electronics apparatus are constructed with transistors, diodes, capacitors and inductors. The modifying factors of these devices are listed in Table I.

As the table shows, the factor π_T is related to temperature, which can be calculated by equation (28). The term T_j is the junction temperature for the transistors and diodes, or the hotspot temperature for the inductors and capacitors. It can be estimated by equation (29), where θ_{JA} is the junction–ambient thermal resistance, P is the loss dissipated by the device, and T_A is the ambient temperature.

The quality factor π_Q is a direct influence factor to the failure rate. Many devices are covered by specifications that have several quality levels.

The environment factor π_E varies with the operational environment, and it is assumed that when the environment is ground benign (GB), $\pi_E=1$.

The application factor π_A varies with the operational power of the device.

The inductance factor π_L varies with the inductor structure. It is assumed that in the case of a fixed inductor structure, $\pi_L=1$.

The capacitor factor π_C varies with the value of the capacitor, which is expressed with microfarads. This factor is expressed in equation (30) where C is the value of the capacitor.

The factor π_V varies with the ratio S between the operating voltage and rated voltage across the capacitor. It can be calculated by equation (31).

The factor π_S varies with the ratio V_S between the reverse voltage and rated reverse voltage across the diode. It can be calculated by equation (32).

$$\pi_T = \exp \left[-A \left(\frac{1}{T_j + 273} - \frac{1}{298} \right) \right] \quad (28)$$

$$T_j = T_A + \theta_{JA} P \quad (29)$$

$$\pi_C = C^{0.23} \quad (30)$$

$$\pi_V = \left(\frac{S}{0.6} \right)^5 + 1 \quad (31)$$

$$\pi_S = V_S^{2.43} \quad (32)$$

Under the same rated power, grid voltage and voltage stress, a comparison of several typical hard-switching transformerless inverter topologies and soft-switching transformerless inverter topologies in terms of reliability is conducted. By assuming that the power switches are MOSFETs IRFP460, the power

diodes are DSEI60-06A, the input DC bus voltage U_i is equal to 360V, and the ambient temperature T_A is 55°C, the factors of the employed devices are listed in Table II, and a comparison of several transformerless PV inverter topologies is shown in Table III.

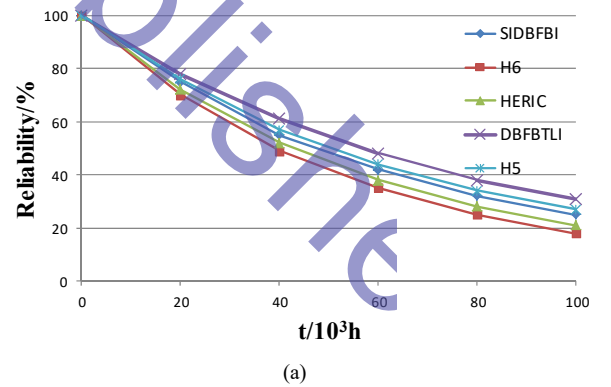
TABLE II
FACTORS OF DEVICES

	Switch	Diode	Capacitor (1n/450p/0.44μ)	Inductor
λ_b	0.012	0.025	0.00012	0.0003
π_T	3.62	7.56	13.36	
π_Q	8	8	10	1
π_E	1	1	1	1
π_A	8			
π_C				1
π_{CV}			0.20/0.16/0.83	
π_V			8.59	
π_S		0.29		
λ_p	2.78	0.44	0.028/0.022/0.11	0.0003

TABLE III
COMPARISON OF SEVERAL TRANSFORMERLESS PV INVERTER TOPOLOGIES

Items	hard-switching transformerless inverter					soft-switching transformerless inverter		
	H5	H6	HERIC C	DBFBFLI [25]	SIDBFBI [24]	SLF-H6-I [14]	ZVT-HERIC [15]	PLSSIDBFBI
Input voltage capacitors	1	1	1	1	1	2	2	1
High-frequency switches	3	2	4	2	2	4	6	2
Low-frequency switches	2	4	2	2	4	4	4	4
Independent diodes	0	2	0	2	2	2	2	8
Filter inductor	2	2	2	2	1	2	2	1
Half-cycle working body diodes	1	0	1	0	0	0	0	0

Comparison results in terms of reliability are shown in Fig. 9. When compared with other hard-switching transformerless inverter topologies, the SIDBFBI topology has only two high-frequency switches, which makes its reliability higher than that of H₅-type topologies, H₆-type topology and the HERIC-type topology, but slightly lower than that of the DBFBFLI topology. However, only one inductor is adopted in the SIDBFBI topology, which economizes the cost. In addition, the saving part of the AC filter can also decrease the volume and weight of the system. The PLSIDBFBI topology proposed in this paper is constructed based on the SIDBFBI. As shown in Fig. 9(b), when compared with other soft-switching transformerless inverter topologies, the snubber circuit of the PLSIDBFBI has no additional active devices, which simplifies the control strategy, facilitates the testing and improves the system reliability.



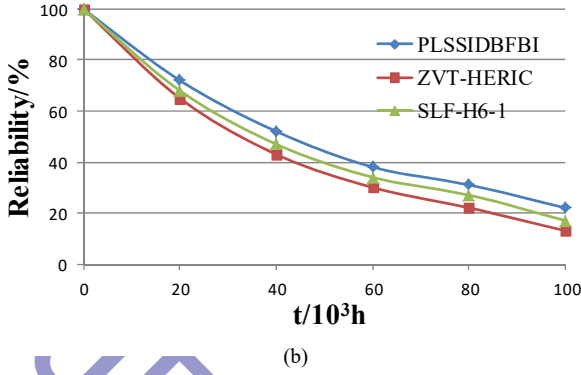


Fig. 9. Comparison of reliability. (a) Hard switching. (b) Soft switching.

V. EXPERIMENTS

An experimental prototype has been built in the laboratory with the listed parameters to further verify the practical operating performance of the proposed inverter: $U_i=360\text{VDC}$, $L=600\mu\text{H}$, $C_f=1\mu\text{f}$, and $u_o=220\text{VAC}/50\text{Hz}$. The controllable switches ($S_1\sim S_4$, S_a , S_b) use power MOSFETs (IPW65R037C6). The power diodes $D_1\sim D_2$ use DSEI60-06A.

From equations (10) and (12), the capacitances and inductances of the snubber circuit can be obtained as: $C_{11}=C_{12}=C_{21}=C_{22}<3.8\text{nF}$ and $L_{11}=L_{22}>10\mu\text{H}$. For experimental testing, the values are set as: $C_{11}=C_{12}=C_{21}=C_{22}=2\text{nF}$ and $L_{11}=L_{22}=50\mu\text{H}$.

From equations (15)-(18) the added snubber circuit increases the conduction loss. However, when compared with the turn-off loss, the increased loss has little influence on the system. Taking the practical conditions into account, the parameters of the snubber circuit are taken as $L_{11\text{max}}<L_{\text{max}}$.

Experimental waveforms of the proposed PLSIDBFBI are shown in Fig. 10. Fig. 10(a) presents part of the driving voltage waveforms, which verify the validity of the adopted high and low frequency modulation strategy. Output waveforms are illustrated in Fig. 10 (b) and Fig. 10 (c). Fig. 10 (b) presents output waveforms at a light load (200W), which shows that the relations of the waveforms and phase are in accordance with the theoretical analysis. The output waveforms at a full load (1008W) shown in Fig. 10 (c) demonstrate that the output waveforms have better performance than those at a light load. Fig. 11 is a comparison of waveforms of the topology with and without a snubber circuit. With the introduction of a snubber circuit, the voltage approaches zero when the power switch is gated off. Therefore, the turn-off loss of the power switch is decreased. When the power switch is gated on, the capacitor and inductor in the snubber circuit resonate and the energy is stored in the snubber circuit. In addition, when the power switch is gated off, the energy is delivered back to load.

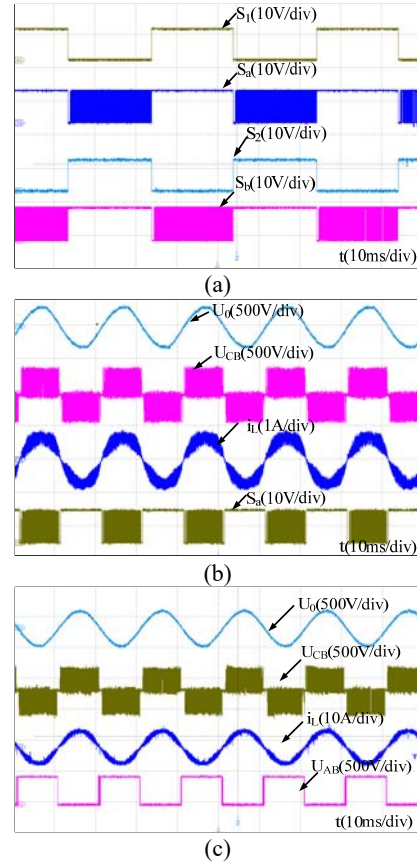


Fig. 10. Experiment waveforms of the passive lossless soft-switching dual buck full bridge inverter.

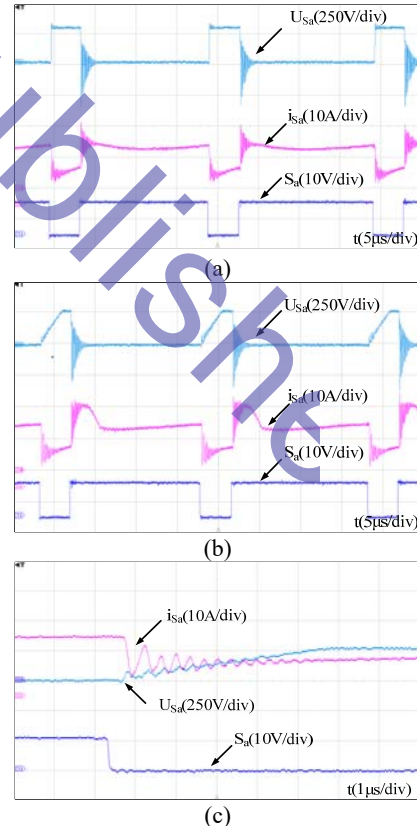


Fig. 11. Comparison of experimental waveforms of switches. (a)

Experimental waveforms of a switch without a snubber circuit. (b) Experimental waveforms of a switch with a snubber circuit. (c) Experimental waveforms of a switch with a snubber circuit.

As analyzed above, the zero-voltage turn-off of high-frequency switches is achieved in the proposed PLSSIDBFBI. In addition, the operating efficiency is improved by delivering stored energy back to the input through snubber circuits. A comparison of the efficiency between several typical transformerless inverters and the PLSSIDBFBI is shown in Fig. 12. As shown in Fig. 12(a), when compared with the SIDBFBI, the snubber circuit in the PLSSIDBFBI reduces the switching loss and increases the system efficiency. The hard-switching transformerless inverters H6 and HERIC have high efficiencies that are slightly below that of the PLSSIDBFBI. However, the previous two inverters possess only a 20 kHz frequency and require a much larger inductor. In addition, as shown in Fig. 12(a), the proposed PLSSIDBFBI produces a higher efficiency at the same frequency when compared with soft-switching SLF-H6-I and ZVT-HERIC. Based on the factors analyzed above, the proposed inverter can achieve both a high efficiency and a decrease in system volume.

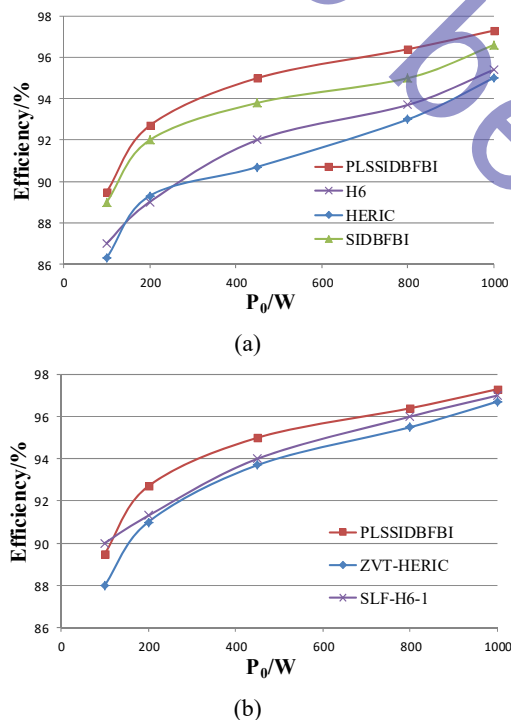


Fig. 12. Comparison of efficiency.

VI. CONCLUSIONS

The novel soft-switching inverter proposed in this paper provides an effective way to increase system efficiency and reliability. According to the above analysis, this inverter has the following features:

1) The advantages of dual buck inverters, such as high conversion efficiency and high reliability, are retained by the

proposed topology. The problems of shoot-through and the reverse recovery of the body diode are removed. In addition, the voltage commutation bridge is adopted to increase the utilization rate of the input voltage and to reduce the voltage stress.

2) When compared with other transformerless inverter topologies, the proposed inverter has only one filter inductor. Therefore, the volume and weight of the system are further decreased, and the integration is more improved.

3) The added snubber circuit realizes lossless soft switching by its own resonance, which simplifies the control strategy, facilitates testing and improves system reliability.

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