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Active Controlled Primary Current Cutting-Off ZVZCS PWM Three-Level DC-DC Converter

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Abstract

A novel active controlled primary current cutting-off zero-voltage and zero-current switching (ZVZCS) PWM three-level dc-dc converter (TLC) is proposed in this paper. The proposed converter has some attractive advantages. The OFF voltage on the primary switches is only Vin/2 due to the series connected structure. The leading-leg switches can obtain zero-voltage switching (ZVS), and the lagging-leg switches can achieve zero-current switching (ZCS) in a wide load range. Two MOSFETs, referred to as cutting-off MOSFETs, with an ultra-low on-state resistance are used as active controlled primary current cutting-off components, and the added conduction loss can be neglected. The added MOSFETs are switched ON and OFF with ZCS that is irrelevant to the load current. Thus, the auxiliary switching loss can be significantly minimized. In addition, these MOSFETs are not series connected in the circuit loop of the dc input bus bar and the primary switches, which results in a low parasitic inductance. The operation principle and some relevant analyses are provided, and a 6-kW laboratory prototype is built to verify the proposed converter.

Key words: Three-level (TL) dc/dc converter, Zero-current switching (ZCS), Zero-voltage switching (ZVS)

I. INTRODUCTION

High input isolated dc-dc converters can be used in many industry applications, such as dc-dc converters for microgrids, distributed power systems, renewable energy power systems and big data centers [1]-[4]. To achieve high system efficiency performance, the DC link voltages of these converters may reach 800V, and sometimes may be even higher than 1000V [2]. To match the voltage rating of the primary switches with widely used low voltage power devices, a lot of three-level (TL) dc-dc converters (TLCs) have been proposed and analyzed [5]. In 1992, the first TLC was reported in [6], which obtains one-half of the voltage stress on each of the primary switches due to the series connected structure. A TLC with no clamping diodes was proposed in [7], which features a simple and compact primary circuit with the same output performance when compared to that of diode-clamped TLC. However, this converter is not suitable for large power applications due to serious input current discontinuity. Some basic TLCs were analyzed and compared in [8]. A full bridge (FB) TLC with a simplified switching scheme was reported in [9], and the primary switches in this converter can obtain zero-voltage switching (ZVS) or zero-current switching (ZCS) in a wide load range. A number of new TLCs were proposed in [10]-[12], which have different advantages. Soft switching schemes of the diode clamped TLC were discussed in [13], and some new wide range soft switching TLCs were also proposed. An asymmetric voltage distribution ZVZCS TLC was proposed in [14], in which hybrids of MOSFETs and IGBTs are used as primary switches because of different voltage distributions on the switching pairs. In [15], a wide range soft switching three-phase TLC was reported, which is well suitable for large power applications. A fault detection and protection scheme for a TLC was discussed in [16]. To reduce the volume of the passive components, some new TLCs with TL secondary rectified voltage waveforms were proposed and discussed in [17]-[19]. All of above mentioned references have made good contributions to this topic.

In [10] and [13], several diode-clamped zero-voltage and zero-current switching (ZVZCS) TLCs were proposed and

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discussed. These TLCs have some common advantages, such as a wide soft switching load range and a simple switching scheme. However, limitations still exist. For the primary current diode cutting-off ZVZCS TLC in [13], two series diodes, referred to as cutting-off diodes, are added to block the reverse primary current, which causes more conduction loss. In addition, the cutting-off diodes are directly inserted into the circuit loop of the primary switches and the input capacitors, which increases the parasitic inductance of the circuit loop. Therefore, large snubber capacitors are needed to absorb the reverse recovery energy during the turn-off instant. A large number of snubber capacitors increases the system volume and causes some heat problems. Thus, the power rating of the primary diode cutting-off ZVZCS TLCs may be limited. For the secondary clamping ZVZCS TLCs in [10] and [13], some secondary reset devices are used to control the current reset instant, and the voltage of the clamping capacitor is applied to the leakage inductance of the transformer to reset the primary current. However, the added active or passive power devices are switched in the hard switching mode, which results in auxiliary switching loss. Furthermore, the current ratings of the active switch and the clamping capacitor are identical to the output current. Thus, this converter is not suitable for large power dc-dc conversions, especially for low output voltage and high output current applications. Hence, it is still a valuable task to find a new ZVZCS TLC for large power applications without the abovementioned problems.

In this paper, a novel active controlled primary current cutting-off ZVZCS PS PWM TLC is proposed. This paper is organized as follows. The configuration and basic operation principle are provided in Section II. Analyzes of the features and a comparison are described in Section III. Experimental results are shown in Section IV. Finally, some conclusions are given in Section V.

II. Configuration and Operation Principle

A. Configuration

Fig. 1 shows the proposed circuit. In the primary side, S_1 to S_4 are series connected, and the OFF voltage on these switches is clamped by D_{cl1} and D_{cl2}. In Fig. 1, the body diodes of S_2 and S_3 are removed since these diodes do not take any effect during operation. However, it should be pointed out that power devices with body diodes can also be used as S_2 and S_3. C_{ss} is a flying capacitor to assist in the ZVS of the leading-leg switches; C_{BL} is a blocking capacitor with a specific value to generate the reset voltage of i_p during the free-wheeling stages; S_5 and S_6 are series MOSFETs referred to as cutting-off MOSFETs in this paper, which are used for cutting-off the primary current during the free-wheeling stages; C_{in1} and C_{in2} are the input capacitors; and L_{lk} is the leakage inductance. In the secondary side, D_{o1} and D_{o2} are the rectifier diodes, and the output filter is composed of L_o and C_o. R_o is the load resistor. The dash line rectangle in Fig. 1 is the circuit loop with a low parasitic inductance requirement. The reduced area of the circuit loop in the dash line rectangle results in a low parasitic inductance, which reduces the voltage spike on the primary switches during the turn-off instant.

B. Operation Principle

Before the analysis, some assumptions are set to simplify the explanation. All of the components in the topology are ideal; C_{in1} and C_{in2} are large enough, and their voltage ripple can be neglected; C_{BL} is designed with a specific value to ensure the ZCS of S_2 and S_3; the output filter and load are replaced by a constant current source I_o; the turn ratio in Fig. 1 is k_T; and C_{os} is the output capacitance of S_1 and S_4. The basic operation principle is provided in Fig. 2. As shown in Fig. 2, four primary switches are switched in the phase-shift (PS) switching scheme. S_1 and S_4 are switched as the leading-leg switches, while S_2 and S_3 are the lagging-leg switches. The duty ratio is represented as D in this paper, and the output voltage is varied from $V_{in}/2k_T$ to 0 with different values of D. There are 14 operation stages in each switching cycle, and the operation stages in the first half switching cycle are depicted in Fig. 3.

Stage 1 [Fig. 3(a)]: Before t_0, the input powers the load. S_1 and S_2 are ON. D_{o2} is conducted while D_{o1} is OFF. S_5 and S_6 are ON, and the added conduction loss is very small because S_5 and S_6 have extremely low on-resistances. The voltage on C_{BL} increases linearly with time and its slope is:

$$\frac{dv_{CBL}}{dt} = \frac{I_o}{k_T C_{BL}} \tag{1}$$

During this stage, $v_{BC}=V_{in}/2-v_{CBL}$; $v_{rect}= (V_{in}/2-v_{CBL})/ k_T$; and $i_P = I_o/k_T$.

Stage 2 [Fig. 3(b), t_0-t_1]: At t_0, S_1 is turned OFF at zero-voltage due to the existence of C_1, v_{CBL} increases and reaches its peak value V_{CBLMAX} at the end of this stage, $i_P=I_o/k_T$, and i_P charges C_1 and discharges C_4 through C_{ss} linearly with time. This stage continues until $v_{C1}= V_{in}/2$ and $v_{C4}=0$. At the end of this stage, D_4 and D_{Cl1} are conducted naturally, the circuit operates in the free-wheeling mode, and both of the rectifier diodes are conducted. S_4 must be gated on to achieve ZVS after t_1.

Stage 3 [Fig. 3 (c), t_1-t_3]: At t_1, D_{cl1} and D_4 are ON, and S_4 is turned on with ZVS at t_2. i_p is free-wheeled through D_{cl1}, S_2 and L_{lk}; and both of the rectifier diodes are conducted. i_P decreases because v_{CBL} is directly applied to L_{lk}, and its expression is:

$$i_P(t) = \frac{I_o}{k_T} - \frac{V_{CBLMAX}}{L_{lk}}(t - t_1) \tag{2}$$

When $i_P=0$, the operation of this stage is finished, and the interval of this stage is:

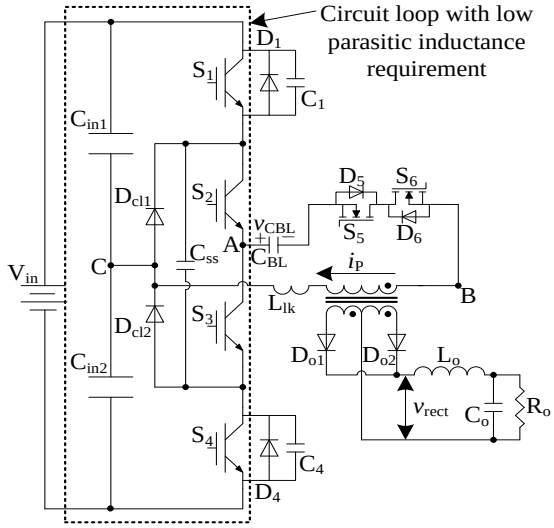

Fig. 1. Active controlled primary current cutting-off ZVZCS PWM TLC.

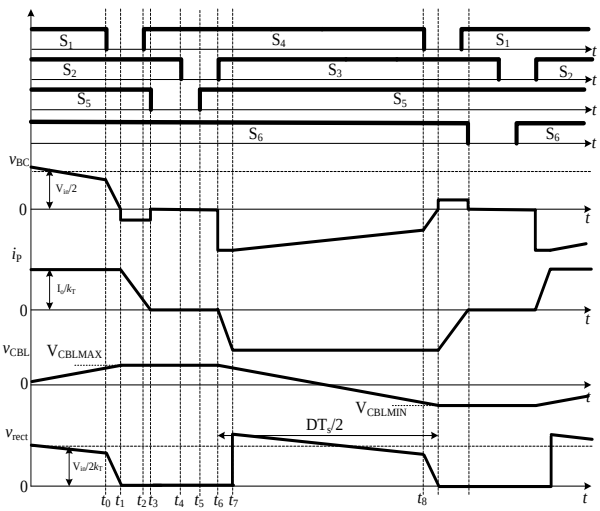

Fig. 2. Basic operation principle.

$$T_{31} = \frac{\mathrm{I_o} L_{\mathrm{lk}}}{k_{\mathrm{T}} \mathrm{V_{CBLMAX}}} \tag{3}$$

Stage 4 [Fig. 3(d), t_3-t_4]: At t_3, i_{P} decays to zero. S_5 is OFF with ZCS. i_{P} cannot flow through the primary coil in the reverse direction because of D_5. After t_3, i_{P} is kept zero. Thus, S_2 can achieve ZCS. The voltage of C_{BL} is kept constant. The voltage on S_5 is V_{CBLMAX}.

Stage 5 [Fig. 3(e), t_4-t_5]: At t_4, S_2 is turned OFF with ZCS. i_{P} is kept zero. The voltage of C_{BL} is kept constant. The voltage on S_5 is V_{CBLMAX}.

Stage 6 [Fig. 3(f), t_5-t_6]: At t_5, S_5 is switched ON with ZCS, and i_{P} is kept zero. The voltage of C_{BL} is kept constant.

Stage 7 [Fig. 3(g), t_6-t_7]: At t_6, S_3 is ON. S_3 can achieve ZCS due to L_{lk}, S_4 is turned on at t_2, i_{P} increases linearly with time in the reverse direction, and the circuit is kept in the free-wheeling mode. i_{P} is:

$$i_{\mathrm{P}}(t) = -\frac{\mathrm{V_{in}}/2 + \mathrm{V_{CBLMAX}}}{L_{\mathrm{lk}}}(t - t_6) \tag{4}$$

During this stage, the voltage of C_{BL} can be treated as a constant value. Therefore, the time of this interval is:

$$T_{76} = \frac{L_{\mathrm{lk}} \mathrm{I_o}}{k_{\mathrm{T}}(\mathrm{V_{in}} + \mathrm{V_{CBLMAX}})} \tag{5}$$

At t_7, i_{P} reaches $-\mathrm{I_o}/k_{\mathrm{T}}$, and the free-wheeling mode is over. The primary powers the load. $v_{\mathrm{BC}}=-\mathrm{V_{in}}/2-v_{\mathrm{CBL}}$; $v_{\mathrm{rect}}=-(\mathrm{V_{in}}/2+v_{\mathrm{CBL}})/k_{\mathrm{T}}$; and $i_{\mathrm{P}} =-\mathrm{I_o}/k_{\mathrm{T}}$. After stage 7, the circuit is operated in the second half switching period.

III. Technical Analysis

A. ZVS of the Leading-Leg Switches

S_1 and S_4 are the leading-leg switches. The leading-leg switches can obtain ZVS in a wide load range because the energy stored in the output inductance can be used. S_4 is selected as an example. The switching instant is shown in Fig. 3(b), and the ZVS criteria for S_4 is:

$$\frac{1}{2} L_{\mathrm{p}}' \left(\frac{\mathrm{I_o}}{k_{\mathrm{T}}}\right)^2 \geq C_{\mathrm{os}} \left(\frac{\mathrm{V_{in}}}{2}\right)^2 \tag{6}$$

Where L_{p}' is equal to $L_{\mathrm{lk}}+k_{\mathrm{T}}^2 L_{\mathrm{o}}$. The minimum load current to realize ZVS for S_4 is:

$$\mathrm{I_{o,min}} = k_{\mathrm{T}} \mathrm{V_{in}} \sqrt{\frac{C_{\mathrm{os}}}{2(L_{\mathrm{lk}} + k_{\mathrm{T}}^2 L_{\mathrm{o}})}} \tag{7}$$

B. ZCS of the Lagging-Leg Switches

S_2 and S_3 are the lagging-leg switches. As verified in [13], with a specific value of C_{BL}, the lagging switches can obtain ZCS in a wide load range. In addition, the value of C_{BL} is [13]:

$$\mathrm{C_{BL}} \leq \frac{(T_{\mathrm{s}} - 2T_{\mathrm{reset}})(T_{\mathrm{reset}} - T_{\mathrm{COM}})}{2L_{\mathrm{lk}}} \tag{8}$$

Where $\mathrm{T_{reset}}$ is the maximum current reset time, and $\mathrm{T_{COM}}$ is the time to allow the tail current of the IGBTs to decrease to zero. During the designing, the load current is set to the rated output current.

C. ZCS of S_5 and S_6

According to Figs. 2 and 3, S_5 and S_6 can obtain ZCS independent of the load current. S_5 is selected as an example. As shown in Figs. 2 and 3(d), S_5 is turned off at t_3, and i_{P} is already reset to zero at this instant. Hence, S_5 can achieve zero-current turn OFF. As shown in Figs. 2 and 3(f), S_5 is turned ON at t_5, and i_{P} is kept zero. Therefore, S_5 can obtain zero-current turn ON.

D. Duty Ratio Loss

The time between t_6 and t_7 in Fig. 2 is defined as the duty ratio loss caused by the leakage inductance, and the corresponding operation stage is plotted in Fig. 3(g). During this interval, i_{P} is:

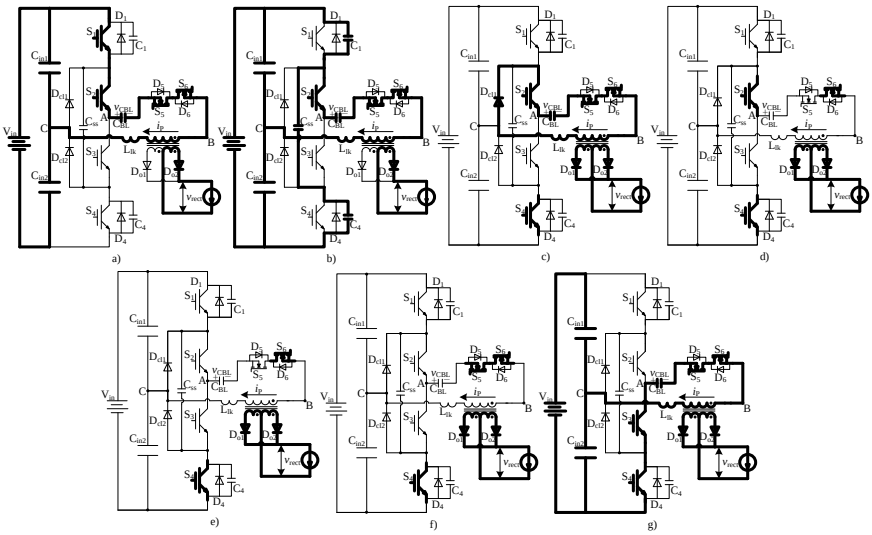

Fig. 3. Operation stages of the proposed converter: (a) stage 1; (b) stage 2; (c) stage 3; (d) stage 4; (e) stage 5; (f) stage 6; (g) stage 7.

$$i_{\mathrm{p}} = -\frac{\mathrm{V_{in}} + V_{\mathrm{CBLMAX}}}{L_{\mathrm{lk}}} \Delta t_{67} \tag{9}$$

In addition, the time of this interval is:

$$\Delta t_{67} = \frac{I_{\mathrm{o}} L_{\mathrm{lk}}}{k_{\mathrm{T}}(\mathrm{V_{in}} + \mathrm{V_{CBLMAX}})} \tag{10}$$

$\mathrm{D_{Loss}}$ is:

$$\mathrm{D_{Loss}} = \frac{\Delta t_{67}}{\mathrm{T_s}/2} = \frac{2 I_{\mathrm{o}} L_{\mathrm{lk}} f_s}{k_{\mathrm{T}}(\mathrm{V_{in}} + \mathrm{V_{CBLMAX}})} \tag{11}$$

Where $\mathrm{D_{Loss}}$ is the duty ratio loss caused by the leakage inductance.

E. Comparison

The proposed converter is compared to conventional ZVZCS TLCs, and the circuits for comparison are presented in Fig. 4. The comparison is based on the following specifications. The input voltage is 600-800V. The output voltage is 12V, and the output current is 500A. The switching frequency is 20-kHz. $\mathrm{V_{CBLMAX}}$ is 50V. 600V/75A IGBTs are used as primary switches. The k_{T} in each converter is 24:1.

Table I shows the added components and added cost as well as a performance comparison. In the proposed converter, two MOSFETs (IPT020N10N3) with extremely low on resistances are required to reset the primary current. In Fig. 4(a), two diodes are series connected with $\mathrm{S_2}$ and $\mathrm{S_3}$. However, since the power losses of these diodes are considerably larger than those of the MOSFETs in the proposed converter, four diodes are required as cutting-off diodes in the converter of Fig. 4(a). As a result of the high current rating of the secondary reset components, the number of active switches and reset capacitors of the converter in Fig. 4(b) are the largest among the three converters. As depicted in Table I, the added cost of the proposed converter is minimum among the three converters.

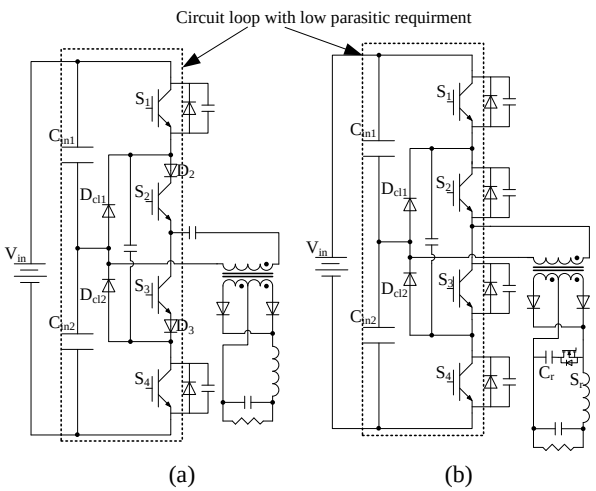

Fig. 4. Conventional ZVZCS TLC. (a) Diode cut-off. (b) Secondary side active reset.

The parasitic inductance among the dc input bus bar and the IGBTs is a key point in high input and high frequency dc-dc power conversion. A large parasitic inductance causes a large over-shoot voltage on the IGBTs during turn-off switching instants, which demands a large value of snubber capacitors to reduce the voltage spike. In addition, snubber capacitors with a large value handle more resonant energy, which causes a thermal problem and reduces the expected lifetime of these capacitors. Hence, the parasitic inductance among the dc input bus bar and the IGBTs should be as low as possible to ensure the safe operation of high input and high frequency dc-dc converters. The dash line rectangles in Figs. 1 and 4 are circuit loops with low parasitic inductance requirements, and the parasitic inductances include the inner parasitic inductances of IGBTs and the parasitic inductances among the input capacitors, lamination bus bar and IGBTs. The layouts of the IGBTs and lamination bus bar of the

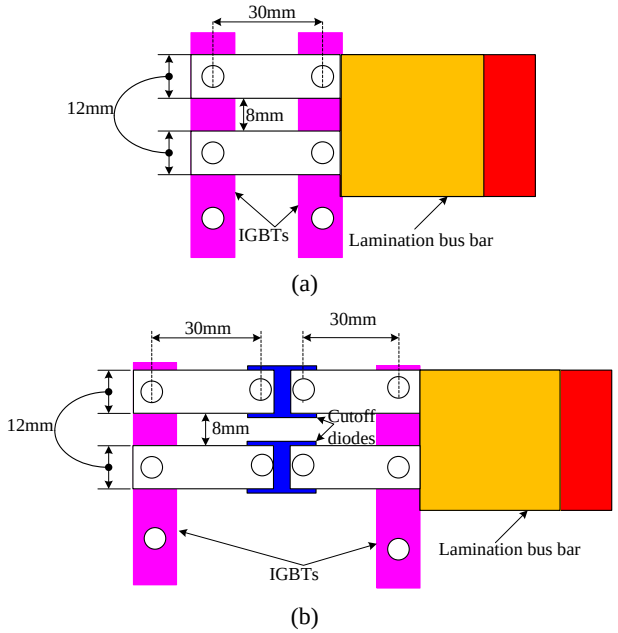

Fig. 5. Layouts of the IGBTs and lamination bus bars for: (a) proposed converter and Fig. 4(b), (b) Fig. 4(a).

TABLE I
ADDED COMPONENTS, ADDED COST AND A PERFORMANCE COMPARISON

Item	Proposed	Fig. 4 (a)	Fig. 4 (b)
Added power electronics devices	Cutting-off MOSFETs (2* IPT020N10N3)	Cutting-off diodes (4* MMF100F20B)	Active reset MOSFETs (5* T020N10N3)
Added passive components	Blocking capacitor (4μF/50A)	Blocking capacitor (4μF/50A)	Reset capacitor (10*0.1μF/100A)
Added cost	$15	$30	$75
Added conduction loss	5W	67W	20W
Added Switching loss	None	None	10W
Parasitic inductance of circuit loop in dash line rectangle	27nH	105nH	27nH

proposed converter and the converters in Fig. 4 are illustrated in Fig. 5. Since the configurations of the primary clamping circuits are identical in these converters, the clamping devices of the primary side are not shown in Fig. 5 for the sake of simplicity. It is clearly the area of a circuit loop with low parasitic inductance requirements in the proposed converter, and the converter in Fig. 4(b) is much lower than that of Fig. 4(a). The values of the parasitic inductances of Fig. 5(a) and (b) are simulated by Ansoft Maxwell, and the parasitic inductance of Fig. 5(a) is about 27nH. However, the total parasitic inductance of Fig. 5(b) is about 105nH. Table I illustrates an added conduction loss comparison. Since two MOSFETs with extremely low on-resistances are used, the total added conduction loss of the proposed converter is much lower than that of Fig. 4.

From the above analyses, it can be concluded that the proposed converter has some clear advantages such as a low parasitic inductance among the dc input bus bar and IGBTs, low added cost, easy designing and manufacturing of the lamination bus bar, smaller value and current stress of the snubber capacitors of the IGBTs, and low added conduction loss.

IV. EXPERIMENTAL RESULTS

A 6-kW laboratory prototype has been built to verify the operation principle of the proposed converter. The main parameters of the prototype are listed in Table II. The switching frequency is set to 20kHz as an example, and the switching frequency for a real product can be further increased. The voltage distribution among the primary switches is similar to those of the converters of [10] and [13]. It is demonstrated in [10] and [13] that the OFF voltage on the primary switches in those converters is even during operation. Therefore, a voltage waveform of the primary switches is not provided in this paper for the sake of simplicity.

Fig. 6 shows the control signals of S_1, S_3, S_4 and S_5. After S_1 is turned OFF, as illustrated in Fig. 6, S_5 is turned off with ZCS at t_1. Before S_3 is turned on, as depicted in Fig. 6, S_5 is turned on with ZCS at t_2.

As shown in Fig. 7, v_{BC} is not a constant value during the power transfer stages because the voltage of the blocking capacitor changes linearly. The dash line circles in Fig. 7 illustrate the primary reset voltage caused by C_{BL}. As shown in Fig. 8, i_P is reset to zero during the freewheeling stages. Thus, the lagging-leg switches can obtain ZCS, and the primary circling current is minimized.

As shown in Fig. 9, v_{CBL} increases or decreases linearly during the power transfer stages, and is kept constant during the free-wheeling stages. The voltage of $v_{S5}+v_{S6}$ is provided in Fig. 10, and it can be concluded that the voltage stress of each cutting-off switch is V_{CBLMAX}. Since V_{CBLMAX} in the prototype is only 50V, MOSFETs with low voltage ratings and extremely low on-resistances can be used as cutting-off switches. Waveforms of v_{Do1} and i_{Lo} are depicted in Figs. 11 and 12.

The soft switching characteristics are depicted in Fig. 13 to Fig. 17. With the parameters of the prototype, the ZVS load ranges of S_1 and S_4 are from 10A to the rated current, and the ZCS load ranges of S_2 and S_3 are below the rated output current. As illustrated in Fig. 13, S_5 is switched ON at t_1, and i_P is kept zero. Therefore, S_5 can obtain zero-current turn on. As shown in Fig. 13, S_6 is switched OFF at t_2, and i_P has already been reset to zero. Thus, S_6 can obtain zero-current

Table II
MAIN PARAMETERS OF THE PROTOTYPE

Item	Parameters
Input	600-800V
Output	12V/500A
Switching frequency	20-kHz
IGBT	MMG75S060B6EN
C_{BL}	3μF/30A
Primary current sensor	25A/100mA
MOSFET driver	MIC4451
L_m	50mH
L_{lk}	10μH
Core type	Toroidal
k_T	24:1
Conductor area of primary coils	8mm^2(enameled wire)
Conductor area of primary coils	125mm^2(copper bar)
S_5 and S_6	IPT020N10N3
Rectifier diodes	MMF400S040DK2B
Synchronous MOSFETs In efficiency test	IPT020N10N3
L_o	2μH

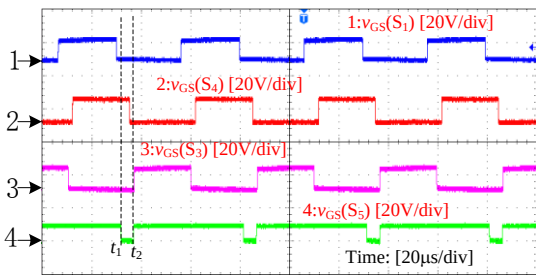

Fig. 6. Control signals of S_1, S_3, S_4 and S_5.

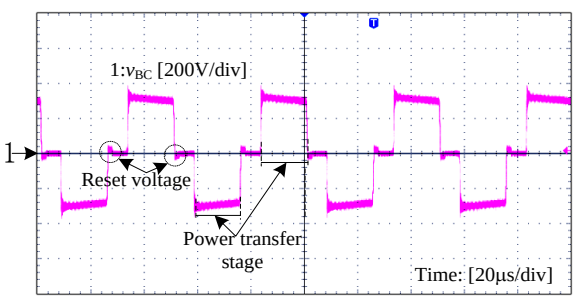

Fig. 7. Waveform of v_{BC}.

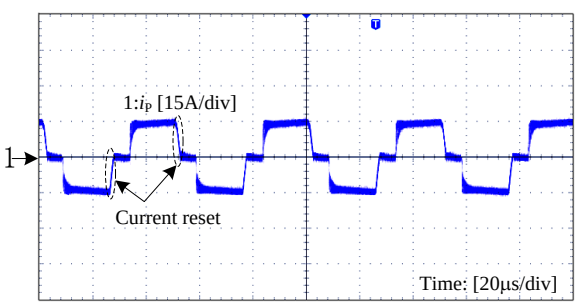

Fig. 8. Waveform of i_P.

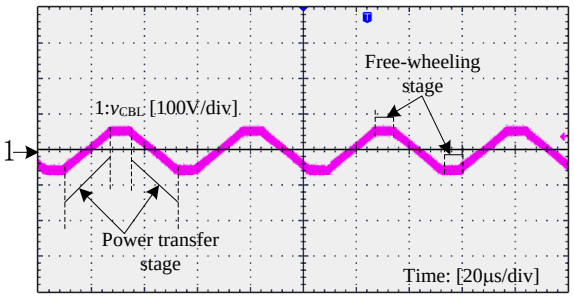

Fig. 9. Waveform of v_{CBL}.

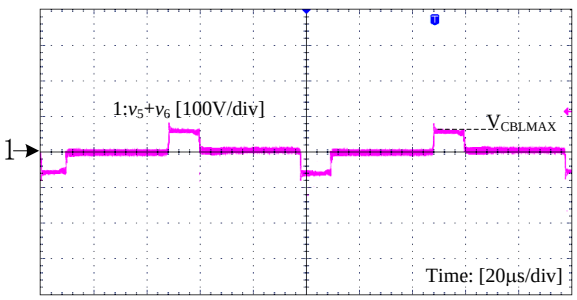

Fig. 10. Waveforms of v_{S5} and v_{S6}.

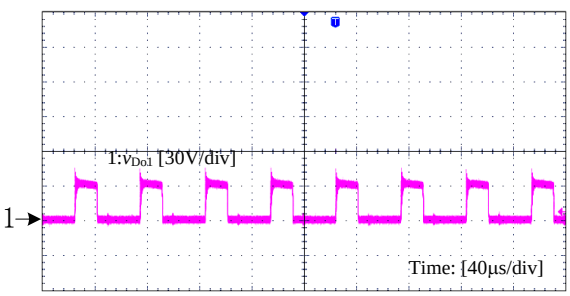

Fig. 11. Waveform of v_{Do1}.

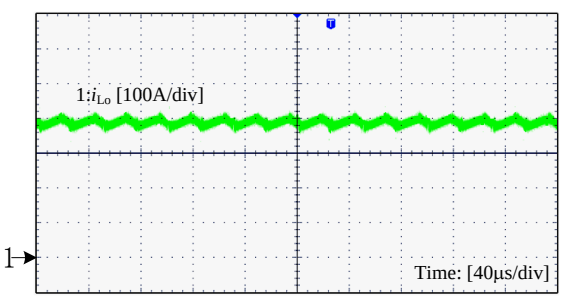

Fig. 12. Waveform of i_{Lo}.

turn OFF. As shown in Fig. 14, v_{CE} (S_3) reaches V_{in} at t_1. However, i_P is still zero. Thus, it can be concluded that S_3 can obtain ZCS. As shown in Fig. 15, v_{GE} (S_1) reaches zero at t_1. However, v_{GE} (S_1) still has a negative value. Thus, S_1 can obtain ZVS operation. From Figs. 16 and 17, it can be concluded that S_4 can obtain ZVS operation, and S_2 can obtain ZCS operation.

In the efficiency test, the converter in Fig. 4(a) is also tested for comparison. Efficiency results are provided in Fig. 18 and the efficiency of the proposed converter with a

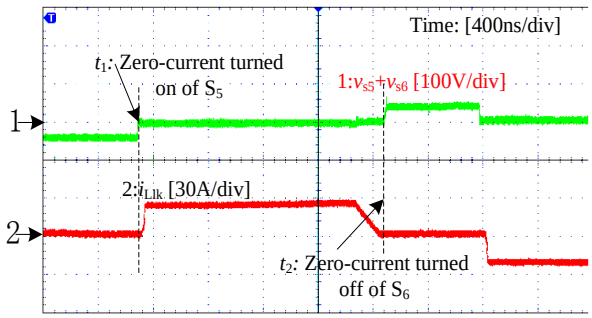

Fig. 13. ZCS of S_5 and S_6.

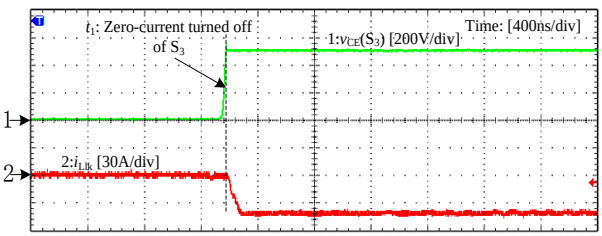

Fig. 14. ZCS of S_3.

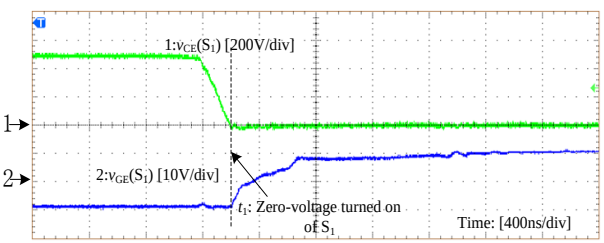

Fig. 15. ZVS of S_1.

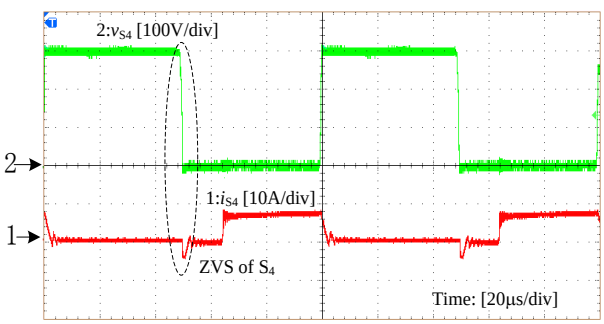

Fig. 16. Waveforms of v_{S4} and i_{S4}.

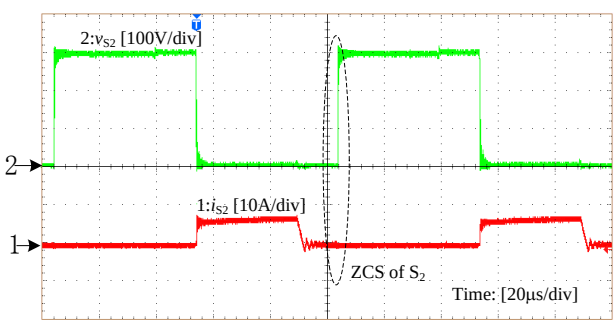

Fig. 17. Waveforms of v_{S2} and i_{S2}.

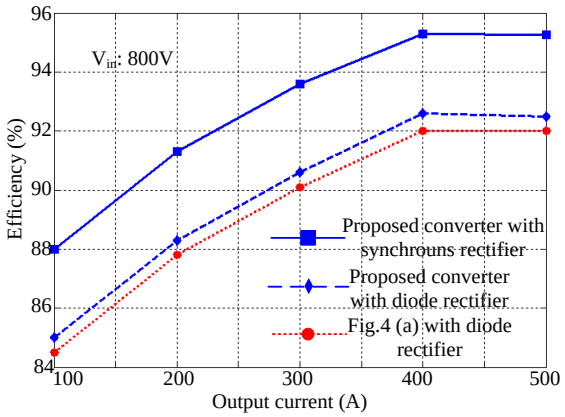

Fig. 18. Efficiency comparison results.

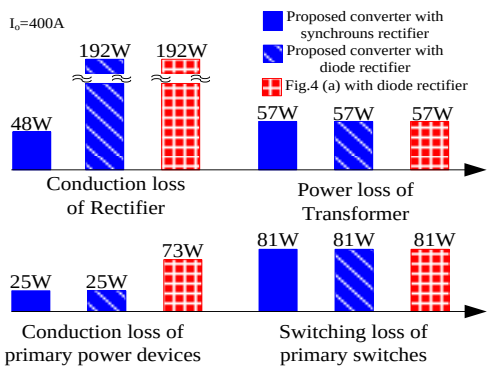

Fig. 19. Main power loss distribution with a 400A load current.

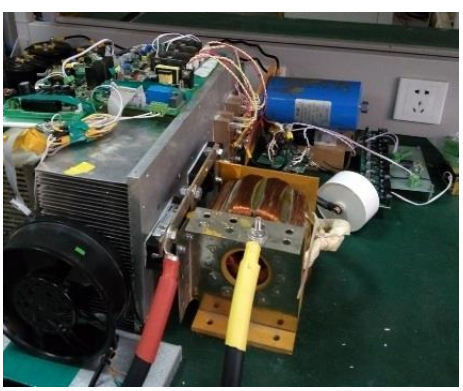

Fig. 20. Photo of the prototype.

synchronous rectifier is shown in Fig. 18. As synchronous rectifier is a well proven technology in power electronics. Thus, the operation principle is not provided here for the sake of the simplicity, and the components used in the synchronous rectifier are depicted in Table II.

The primary switches, rectifier diodes and output filters used in Figs. 1 and 4(a) are identical to the parameters in Table II. 4×MMF100F20B are used as cutting-off diodes in Fig. 4(a). The power loss of the rectifier, the auxiliary power to the controller and the driver are taken into account in the efficiency test. As shown in Fig. 18, the efficiency of the proposed converter is a little higher than that of the converter

in Fig. 4 due to a reduced added conduction loss. The output voltage is only 12V, as shown in Fig. 18. Thus, a synchronous rectifier may be a better choice. The main power loss distribution with 400A load current is depicted in Fig. 19. Fig. 20 shows a photo of the prototype.

V. CONCLUSIONS

A novel active controlled primary current cut-off ZVZCS TLC is proposed in this paper. The theoretical analysis is verified with a 6-kW laboratory prototype. The improvements of the proposed converter are listed as follows: the leading-leg switches can obtain zero-voltage switching (ZVS) and the lagging-leg switches can achieve zero-current switching (ZCS) in a wide load range; two MOSFETs with extreme low on-resistances are used as primary current active controlled cutting-off components, and the maximum added conduction loss is only about 0.05% of the rate power; the active controlled cutting-off MOSFETs are switched ON and OFF with ZCS, and there are no added switching losses; and the added MOSFETs are not series connected in the circuit loop of the dc lamination input bus bar and IGBTs, which results in lower parasitic inductances among the dc input lamination bus bar and IGBTs. Finally, the cost of the added components is only about 1.25% of the total cost. Therefore, the proposed converter is a promising solution for high input and high frequency large power dc-dc conversion.

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